Application Note

What is a Power MOSFET?

General description of power MOSFETs and our power MOSFET products

Contents

1. Description

This document provides a general description of power MOSFETs. For more information on our power MOSFET products, please refer to the links below.

- **Power MOSFETs**
  https://www.semicon.sanken-ele.co.jp/ctrl/en/product/category/MOSFET/

2. Power MOSFETs

2.1. What is a power MOSFET?

A power MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is a field-effect transistor with a MOS structure. The structure of power MOSFETs is classified into horizontal type and vertical type, and the main products of our power MOSFETs are vertical type. Vertical type is classified into planar type and trench type.

Figure 2-1 shows an example of a section view of a planar power MOSFET (N-channel). This document describes a planar power MOSFET (N-channel) as an example. In vertical power MOSFETs in which the current flows in the vertical direction, the on-resistance per chip area is reduced because of miniaturization.

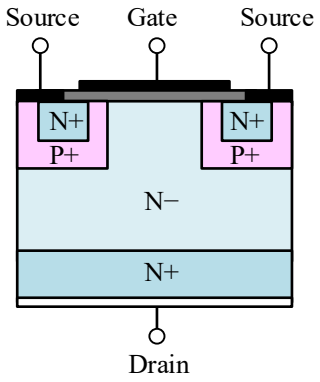
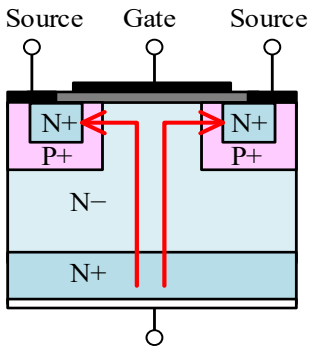
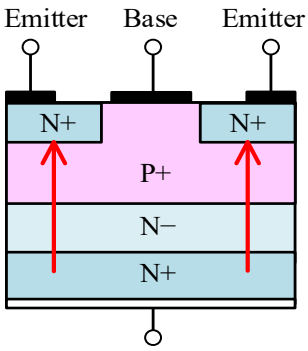
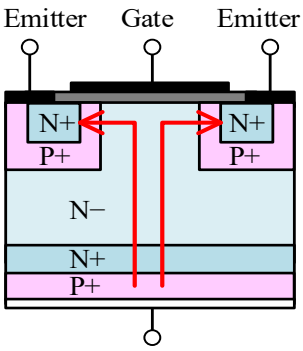
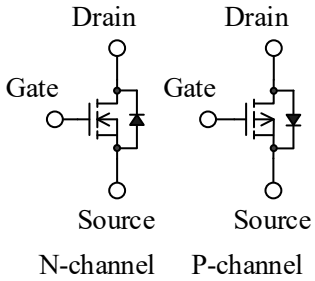
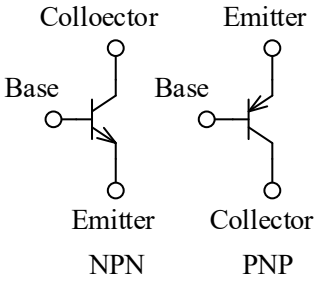
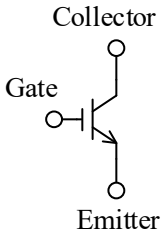


Figure 2-1. Section View Example of a Planar Power MOSFET (N-channel)

2.2. Features of Power MOSFETs

The features of power MOSFETs when compared with bipolar transistors and IGBTs are shown below.

Item	Power MOSFET	Bipolar Transistor	IGBT
Structure (arrows indicate the direction of the drain current / collector current)			
Circuit Diagram			
Control Systems	Voltage control	Current control	Voltage control
Driving Power	Small	Large	Small
Switching Speed	Fast	Slow	Medium
Breakdown Voltage	About 30 V to 800 V	About 50 V to 800 V	About 400 V to 1200 V
Increasing the Current	Easy (about 1 A to 100 A)	Difficult (about 2 A to 25 A)	Easy (about 15 A to 40 A)
Applications	● Low Stepping Motor ● Low-voltage/high-voltage brushless DC motor ● Switching power suply	● Audio ● Low-voltage/high-voltage brushless DC motor ● Solenoid	● High-voltage brushless DC motor ● Inverter

2.3. Absolute Maximum Ratings

The absolute maximum ratings are defined as the allowable limits that should not be exceeded, even instantaneously. If one or more of these values are exceeded, the semiconductor device will break. Therefore, it is required to design electronic devices that use semiconductors so that the stress exceeding the values is not applied to semiconductors even instantaneously.

Absolute maximum ratings do not guarantee reliability. Even within the absolute maximum ratings, if the recommended conditions are exceeded, their durability decreases and as a result, semiconductors may not withstand long-term use.

Typical characteristics of the absolute maximum ratings listed in the power MOSFET data sheet are shown below. The parameters of absolute maximum ratings listed depend on the power MOSFET type.

Parameter	Symbol	Description	Remarks
Drain-to-Source Voltage	V_{DS}	Maximum voltage that can be applied between drain and source	
Gate-to-Source Voltage	V_{GS}	Maximum voltage that can be applied between gate and source	Section 2.4.2
Drain Current (DC)	I_D	Maximum current that can flow continuously in the drain pin	
Drain Current (pulse)	I_{DM}	Maximum current that can flow in the drain pin for a short time	
Source-to-Drain Body Diode Forward Current (DC)	I_S	Maximum current that can flow continuously in the body diode	
Source-to-Drain Body Diode Forward Current (pulse)	I_{SM}	Maximum current that can flow through the body diode for a short time	
Avalanche Energy	E_{AS}	Allowable maximum energy at avalanche breakdown by applying a single pulse	Section 2.6.1.1
Avalanche Current	I_{AS}	Maximum current that can flow at avalanche breakdown	Section 2.6.1.1
Maximum Drain-to-Source dv/dt	dv/dt1	Allowable maximum voltage change rate between drain and source	
Maximum Diode Recovery dv/dt	dv/dt2	Allowable maximum voltage change rate at body diode reverse recovery	
Maximum Diode Recovery di/dt	di/dt	Allowable maximum current change rate at body diode reverse recovery	
Power Dissipation	P_D	Allowable maximum power dissipation	
Operating Junction Temperature	T_J	Allowable maximum temperature in the semiconductor junction in the product	
Storage Temperature	T_{STG}	Temperature range at which the product can be stored when the device is not operating	

2.4. Electrical Characteristics

Electrical characteristics show the performance of a product by specifying conditions such as temperature, voltage, and current.

The following are typical parameters of electrical characteristics described in the data sheet. The parameters of electrical characteristics to be listed depend on the type of power MOSFETs.

Parameter	Symbol	Description	Remarks
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	Breakdown voltage between drain and source	Section 2.4.1
Drain-to-Source Leakage Current	I_{DSS}	Drain leakage current when the gate voltage is 0 V	
Gate-to-Source Leakage Current	I_{GSS}	Gate leakage current when the gate voltage is under the specified conditions	
Gate Threshold Voltage	$V_{GS(TH)}$	The gate voltage when the power MOSFET turns on and the drain current starts to flow	Section 2.4.2
Drain-to-Source On-resistance	$R_{DS(ON)}$	Resistance between drain and source when the drain current is flowing	Section 2.4.3
Internal Gate Resistor	$R_{G(INT)}$	Gate resistor inside the power MOSFET	
Input Capacitance	C_{iss}	Sum of gate-to-drain capacitance and gate-to-source capacitance	Section 2.4.4
Output Capacitance	C_{oss}	Sum of gate-to-drain capacitance and drain-to-source capacitance	
Reverse Transfer Capacitance	C_{rss}	Capacitance between gate and drain	
Total Gate Charge	Q_G	Total charge that the gate voltage increases to the specified voltage from 0 V	Section 2.4.5
Gate-to-Source Charge	Q_{GS}	The charge that the gate voltage reaches mirror voltage from 0 V	
Gate-to-Drain Charge	Q_{GD}	The charge from when the gate voltage reaches the mirror voltage to when the drain-to-source voltage ≈ 0 V (the charge during the mirror period)	
Turn-on Delay Time	$t_{d(ON)}$	Delay time until the power MOSFET turns on	Section 2.4.6
Turn-on Rise Time	t_r	Rise time until the power MOSFET turns on	
Turn-off Delay Time	$t_{d(OFF)}$	Delay time until the power MOSFET turns off	
Turn-off Fall Time	t_f	Fall time until the power MOSFET turns off	
Source-to-Drain Body Diode Forward Voltage Drop	V_{SD}	Voltage drop when forward current flows through the body diode	Section 2.4.7
Source-to-Drain Body Diode Reverse Recovery Time	t_{rr}	Time from when the recovery current flows through the body diode to when the recovery current recovers to 90% of the peak value	Section 2.4.7
Source-to-Drain Body Diode Reverse Recovery Charge	Q_{rr}	The charge of flowing current at reverse recovery time	Section 2.4.7

2.4.1. Drain-to-Source Breakdown Voltage, $V_{(BR)DSS}$

$V_{(BR)DSS}$ is the breakdown voltage between the drain and source. The electrical characteristics are specified in the minimum value, and a margin is applied for the actual value for the safety of circuit operation. However, there is a trade-off relationship between $V_{(BR)DSS}$ and drain-to-source on-resistance, $R_{DS(ON)}$, thus, increasing the margin of $V_{(BR)DSS}$ also increases $R_{DS(ON)}$. Therefore, the margin of $V_{(BR)DSS}$ is generally designed to be as small as possible. $V_{(BR)DSS}$ has a positive temperature coefficient, and the higher the temperature, the higher the $V_{(BR)DSS}$. The circuit should be designed considering that the $V_{(BR)DSS}$ becomes low at low temperatures.

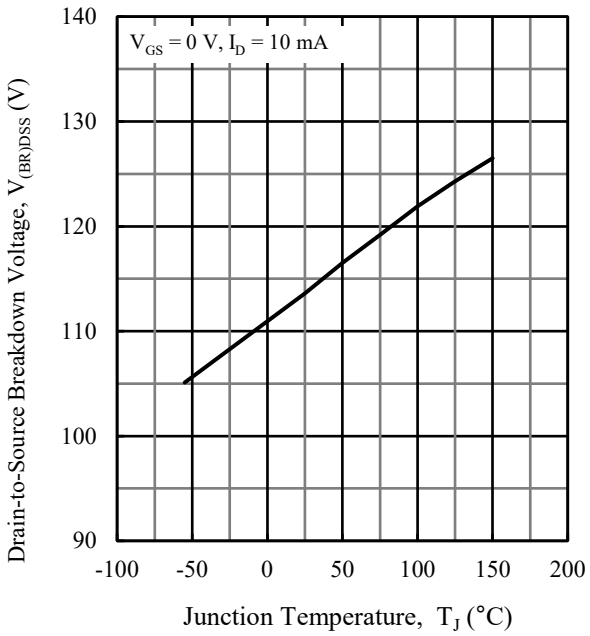


Figure 2-2. $V_{(BR)DSS}$ – T_J Typical Characteristics

2.4.2. Gate Threshold Voltage, $V_{GS(TH)}$

$V_{GS(TH)}$ is the voltage between gate and source when the power MOSFET turns on and the drain current, I_D, starts to flow. $V_{GS\ (TH)}$ has a negative temperature coefficient, and the higher the temperature, the lower the $V_{GS\ (TH)}$ (see Figure 2-3). The temperature becomes high during circuit operation and the power MOSFET turns on at a low voltage. Therefore, changes in $V_{GS\ (TH)}$ due to temperature characteristics must be taken into account in designing the circuit in order to avoid malfunction due to noise.

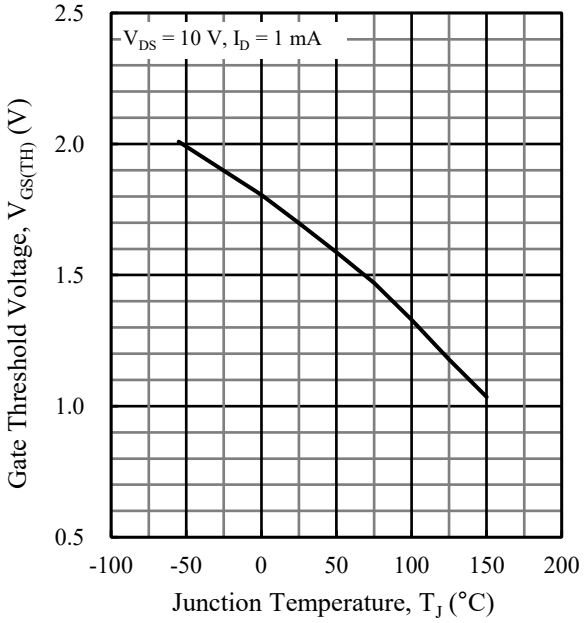


Figure 2-3. $V_{GS(TH)}$ – T_J Typical Characteristics

V_{GS} is the applied voltage between gate and source. In order to control the drain current, I_D, with V_{GS}, check the I_D – V_{GS} characteristics described in the data sheet and set the V_{GS} so that the required I_D can flow (see Figure2-4).

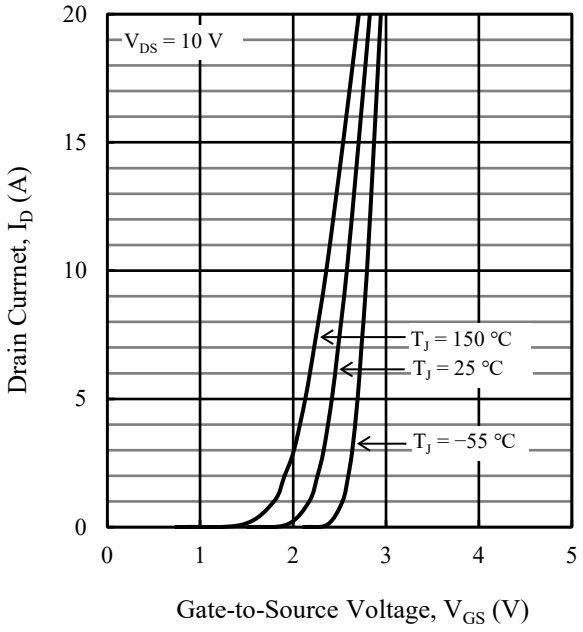


Figure2-4. I_D – V_{GS} Typical Characteristics

2.4.3. Drain-to-Source On-resistance, $R_{DS(ON)}$

$R_{DS\,(ON)}$ is the resistance between the drain and source when the drain current, I_D, is flowing. The larger the $R_{DS(ON)}$, the larger the power loss. Therefore, a power MOSFET with small $R_{DS(ON)}$ is ideal. $R_{DS(ON)}$ has a positive temperature coefficient, and the higher the temperature, the higher the $R_{DS(ON)}$ (see Figure 2-5). When using at high temperature, consider the change in $R_{DS(ON)}$ due to temperature characteristics. When power MOSFETs are connected in parallel, if there are variations in each $R_{DS(ON)}$, a large amount of current flows through the power MOSFETs with small $R_{DS(ON)}$. However, the flowing current decreases because the $R_{DS(ON)}$ increases due to the temperature rises. The current flowing through each power MOSFET is balanced without the current flowing concentrated on one power MOSFET. This is called the self-stabilizing function of the power MOSFET.

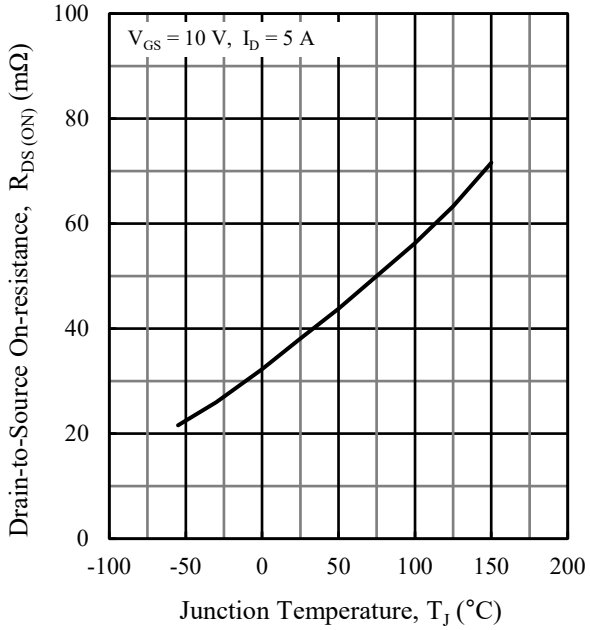


Figure 2-5. $R_{DS(ON)}$ – T_J Typical Characteristics

- **$R_{DS(ON)}$ Resistance**

Figure 2-6 shows the $R_{DS(ON)}$ resistance of the planar power MOSFET (N-channel).

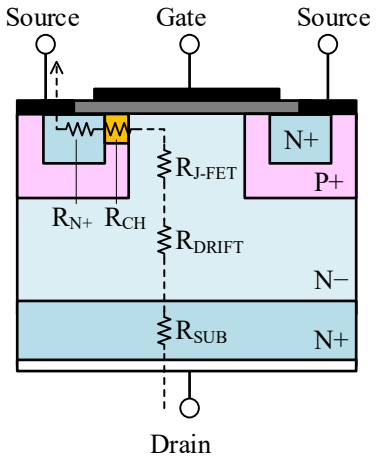


Figure 2-6. $R_{DS(ON)}$ Resistance of the Planar Power MOSFET (N-channel)

$R_{DS(ON)}$ resistance is calculated by the following equation.

$$R_{DS(ON)} = R_{SUB} + R_{DRIFT} + R_{J-FET} + R_{CH} + R_{N+}$$

Where:
R_{SUB} is substrate resistance,
R_{DRIFT} is drift resistance,
R_{J-FET} is J-FET resistance,
R_{CH} is channel resistance, and
R_{N+} is N+ layer resistance.

There is a trade-off relationship between breakdown voltage and $R_{DS(ON)}$, thus, increasing the breakdown voltage also increases $R_{DS(ON)}$. In order to increase the breakdown voltage of the power MOSFET, it is required to thicken the N− layer shown in Figure 2-6. Therefore, the $R_{DS(ON)}$ of a high breakdown voltage power MOSFET depends on the drift resistance, R_{DRIFT}. Conversely, the $R_{DS(ON)}$ of a low breakdown voltage power MOSFET depends more on the channel resistance, R_{CH}, than on R_{DRIFT}.

2.4.4. Capacitance Characteristics (C_{iss}, C_{oss}, C_{rss})

As shown in Figure 2-7, due to the structure of power MOSFETs, parasitic capacitances (C_{GS}, C_{GD}, C_{DS}) are generated. These parasitic capacitances affect the switching characteristics.

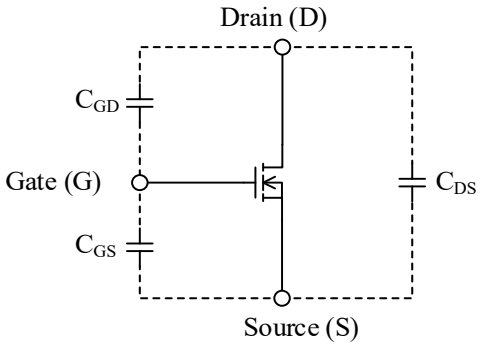


Figure 2-7. Parasitic Capacitances of Power MOSFET

● **Input Capacitance, C_{iss}**

Input capacitance, C_{iss}, affects the delay time. When the C_{iss} is large, the delay time is long because a large amount of charge must be charged/discharged at the power MOSFET turning on/off. The larger the C_{iss}, the larger the power loss. Therefore, the power MOSFET with small C_{iss} is ideal.

C_{iss} is calculated by the following equation.

$$C_{iss} = C_{GS} + C_{GD}$$

● **Output Capacitance, C_{oss}**

The output capacitance, C_{oss}, affects the turn-off characteristics. When the C_{oss} is large, the voltage change rate, dv/dt, of the drain-to-source voltage, V_{DS}, is reduced at the power MOSFET turn-off, resulting in reducing the influence of noise but increasing the turn-off fall time, t_f.

C_{oss} is calculated by the following equation.

$$C_{oss} = C_{DS} + C_{GD}$$

● **Reverse Transfer Capacitance, C_{rss}**

Reverse transfer capacitance, C_{rss} is also called mirror capacitance.

C_{rss} affects high frequency characteristics. The larger the C_{rss}, the more the following characteristics appear.

- The fall time of drain-source voltage, V_{DS}, at turn-on is long
  (The turn-on rise time, t_r is long)
- The rise time of drain-source voltage, V_{DS}, at turn-off is long
  (The turn-off fall time, t_f is long)
- Power loss is large

Reverse transfer capacitance, C_{rss} is calculated by the following equation.

$$C_{rss} = C_{GD}$$

2.4.5. Charge Characteristics (Q_G, Q_{GS}, Q_{GD})

Total Gate Charge, Q_G, gate-to-source charge, Q_{GS}, and gate-to-drain charge, Q_{GD}, are the charges required to drive the power MOSFET (see Figure 2-8). These affect the switching characteristics. The smaller the value, the smaller the power loss, and the fast switching is achieved.

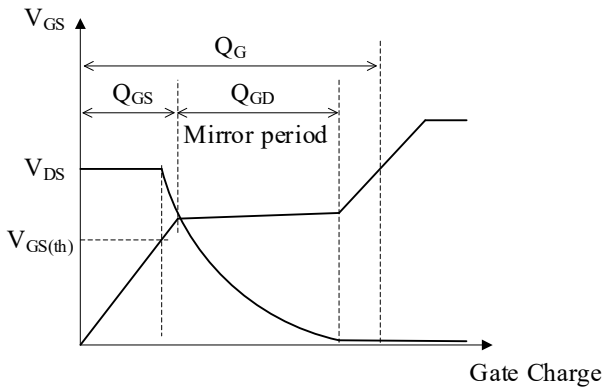


Figure 2-8. Relationship between V_{GS} and Gate Charge

2.4.6. Switching Characteristic ($t_{d(ON)}$, t_r, $t_{d(OFF)}$, t_f)

Figure 2-9 shows the definition of switching time.

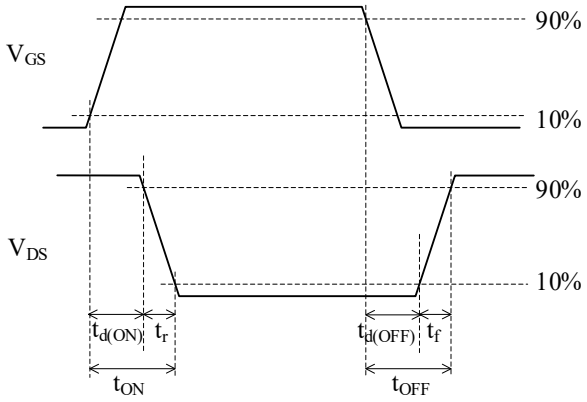


Figure 2-9. Definition of Switching Time

- **Turn-on Delay Time, $t_{d(ON)}$**
  Time from 10% of the V_{GS} setting value to 90% of the V_{DS} setting value

- **Turn-on Rise Time, t_r**
  Time from 90% to 10% of the V_{DS} setting value

- **Turn-on Time, t_{ON}**
  The total time of $t_{d(ON)}$ and t_r.

- **Turn-off Time, $t_{d(OFF)}$**
  Time from 90% of the V_{GS} setting value to 10% of the V_{DS} setting value

- **Turn-off Fall Time, t_f**
  Time from 10% to 90% of the V_{DS} setting value

- **Turn-off Time, t_{OFF}**
  The total time of $t_{d(OFF)}$ and t_f.

2.4.7. Body Diode

Due to the structure of power MOSFETs, a body diode is generated between the source and drain. Figure 2-10 shows the I_S – V_{SD} characteristics of the body diode. The V_{SD} has a negative temperature characteristic and thus the higher the temperature, the lower the V_{SD}.

Figure 2-11 shows the reverse recovery characteristics of the body diode. The peak recovery current is defined as I_{RM}. The smaller the reverse recovery time, t_{rr}, and the reverse recovery charge, Q_{rr}, the smaller the power loss.

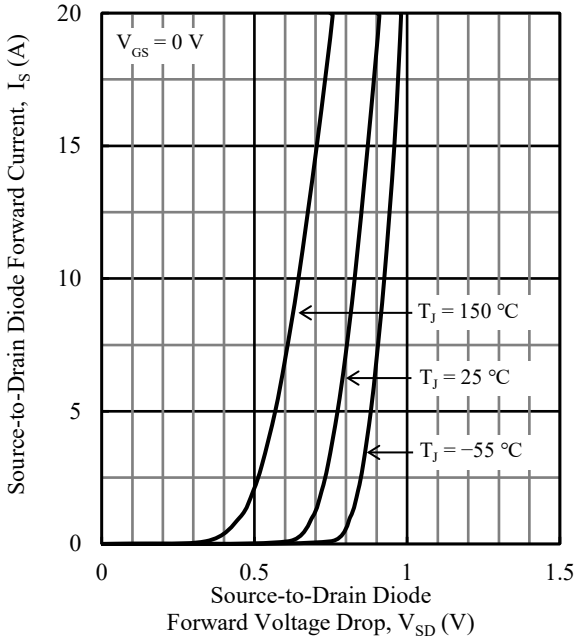


Figure 2-10. I_S – V_{SD} Typical Characteristics

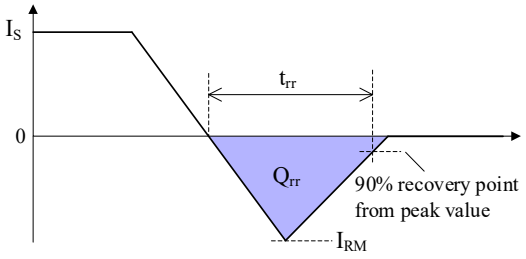


Figure 2-11. Reverse Recovery Characteristics

2.5. Thermal Characteristic

The following are typical parameters of thermal characteristics described in the data sheet. The parameters of thermal characteristics to be listed depend on the type of power MOSFET.

Parameter	Symbol	Description
Thermal Resistance	$R_{\theta JC}$	Thermal resistance between semiconductor junction and case
	$R_{\theta JA}$	Thermal resistance between semiconductor junction and ambient

2.6. Factors that Cause Power MOSFET Destruction

Power MOSFETs are destroyed mainly by the following five factors.

- Destruction by Avalanche Breakdown
- SOA Destruction
- Body Diode Destruction
- Destruction by Parasitic Oscillation
- Destruction by ESD

2.6.1. Destruction by Avalanche Breakdown

Avalanche breakdown occurs when the drain-to-source voltage exceeds the absolute maximum rating to be breakdown voltage, $V_{(BR)DSS}$, or higher. In the breakdown region, the power MOSFET may be destroyed due to the following factors.

- **Destruction by Current**

Figure 2-12 shows a section view of a planar power MOSFET (N-channel). In the breakdown region, the avalanche current, I_{AS}, flows as shown in (A) in Figure 2-12. At this time, a voltage is generated across the base resistor, R_B, of the parasitic NPN bipolar transistor. When the voltage exceeds the base-to-emitter voltage that turns on the parasitic NPN bipolar transistor, a current flows as shown in (B) in Figure 2-12. At this time, if the drain-to-source voltage is high, the secondary breakdown occurs in the parasitic NPN bipolar transistor, thus, the current flowing through the transistor increases rapidly, resulting in the destruction of power MOSFET.

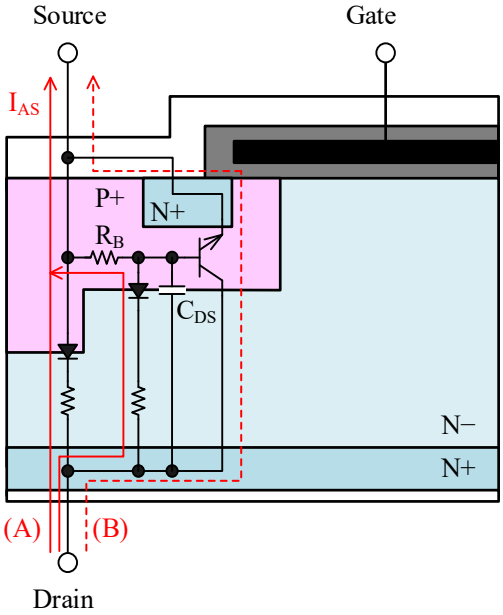


Figure 2-12. Section View of a Planar Power MOSFET (N-channel)

- **Destruction by Energy**

The power dissipation of energy due to avalanche breakdown causes the temperature to rise. When the junction temperature, T_J, exceeds the absolute maximum rating, the power MOSFET is destroyed.

● **Decrease in Destruction Capability due to dv/dt**

As shown in Figure 2-13, a power MOSFET generates parasitic capacitance, C_{DS}, between drain and source.

As shown in (A) in Figure 2-13, the current, I, flows at the power MOSFET turn-off. The current, I, can be calculated by the following equation.

$$I = C_{DS} \times dv/dt$$

Where:
C_{DS} is parasitic capacitance, and
dv/dt is change rate of rise of drain-to-source voltage, V_{DS}

At this time, a voltage ($R_B \times I$) is generated across the base resistor ,R_B, of the parasitic NPN bipolar transistor. When this voltage exceeds the base-to-emitter voltage that turns on the parasitic NPN bipolar transistor, a current flows as shown in (B) in Figure 2-13. As a result, the destruction capability is decreased.

Note that the larger the dv/dt at power MOSFET turn-off, the larger the flowing current, I, and thus, the parasitic NPN bipolar transistor easily turns on.

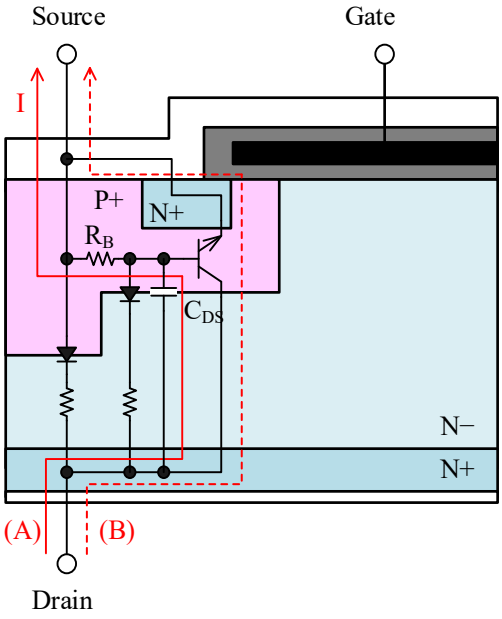


Figure 2-13. Section View of a Planar Power MOSFET (N-channel)

● **Measures**

The following measures are effective in suppressing the destruction caused by the avalanche breakdown.

- The wiring should be as wide and short as possible to reduce the stray inductance.
- The value of the external gate resistor should be large and dv/dt should be small.
- A snubber circuit or a Zener diode should be connected between drain and source to absorb the surge voltage.

2.6.1.1. Avalanche Energy Measurement

When the drain-to-source voltage exceeds the absolute maximum rating and increases to the breakdown voltage, $V_{(BR)DSS}$, or higher at the power MOSFET turn-off in the inductive load circuit, avalanche breakdown occurs. The current that flows at this time is called the avalanche current, I_{AS}, and the generated energy is called the avalanche energy, E_{AS}.

Figure 2-14 shows the avalanche energy measurement circuit. Figure 2-15 shows the switching waveforms.

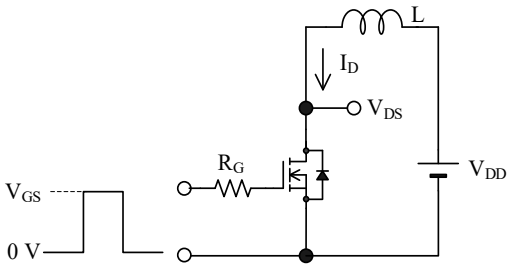


Figure 2-14. Avalanche Energy Measurement Circuit

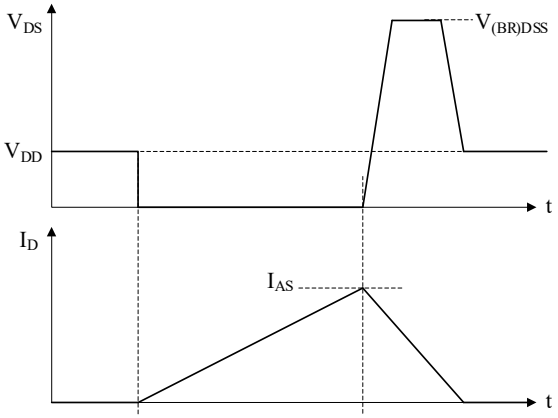


Figure 2-15. Switching Waveform

Avalanche energy, E_{AS}, is calculated by the following equation.

$$E_{AS} = \frac{1}{2} \times L \times {I_{AS}}^2 \times \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}$$

Where:
E_{AS} is avalanche energy (J),
V_{DD} is power supply voltage (V),
L is inductance (H),
I_{AS} is avalanche current (A), and
$V_{(BR)DSS}$ is drain-to-source breakdown voltage (V).

2.6.2. SOA Destruction

If any of the maximum rating of drain current, the maximum rating of drain-to-source voltage, V_{DS}, and the maximum rating of junction temperature exceeds the safe operating area, the power MOSFET may generate abnormal heat, resulting in power MOSFET destruction. See Section 2.6.2.1 for the safe operating area.

2.6.2.1. Safe Operating Area (SOA)

The Safe Operating Area (SOA) is the range of current and voltage that a power MOSFET can be used without deterioration or destruction. The safe operating area is divided by the following limits.

(1) The area limited by the maximum rated value of drain current
(2) The area limited by the maximum value of on-resistance, $R_{DS(ON)}$
(3) The area limited by the maximum rated value of junction temperature
(4) The area limited by the secondary breakdown
(5) The area limited by the maximum rated value of drain-to-source voltage, V_{DS}

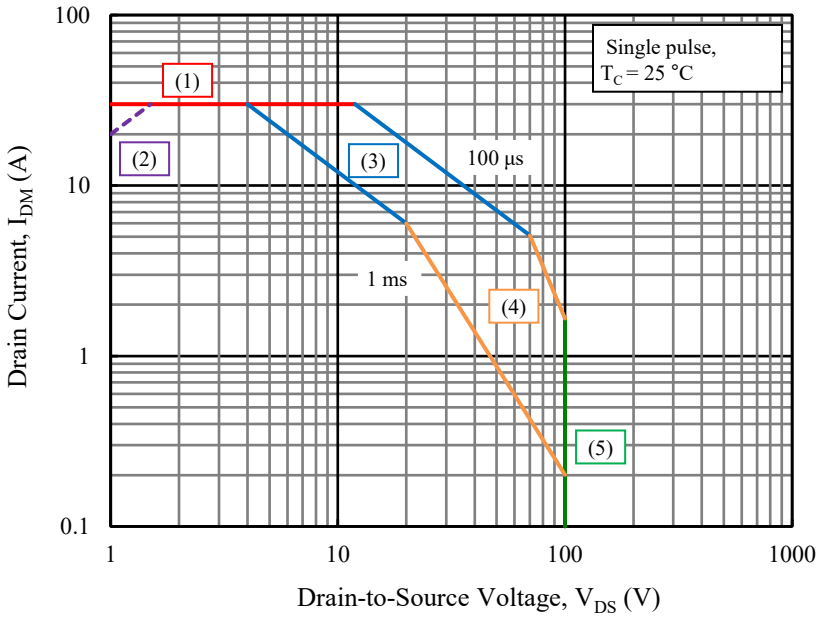


Figure 2-16. Example of Safe Operating Area

The data sheet describes the safe operating area under the ideal conditions (single pulse, T_C = 25 °C, etc.). Use the power MOSFET within the safe operating area by derating the graph to the actual operating conditions. For derating, refer to the following URL.

https://www.semicon.sanken-ele.co.jp/en/support/reliability/4-5.html#sec2

2.6.3. Body Diode Destruction

In a circuit that a body diode between source and drain is intentionally used, when the current change rate (di/dt) at the body diode reverses recovery is steep, the voltage change rate (dv/dt2) at this time is also steep. At this time, the parasitic NPN transistor inside the power MOSFET turns on and current flows, which may result in destruction of the power MOSFET.

● **Measures**

- The wiring should be as wide and short as possible to reduce the stray inductance.
- The value of the external gate resistor should be large and dv/dt2 should be small.
- A snubber circuit or a Zener diode should be connected between drain and source to absorb the surge voltage.

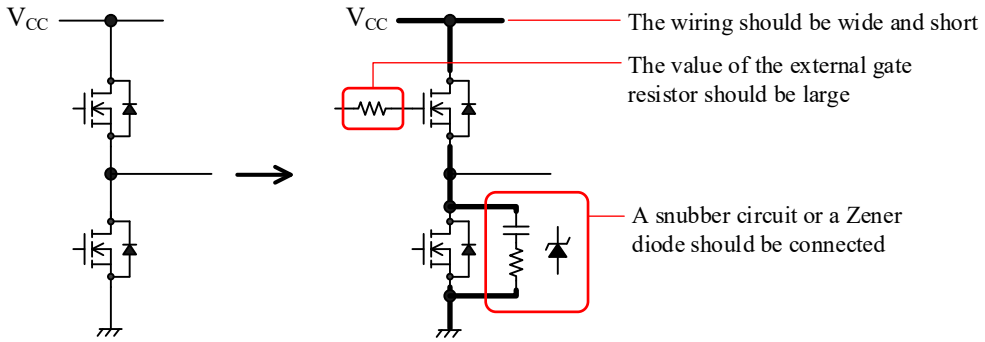


Figure 2-17. Body Diode Destruction Measure Example

2.6.4. Destruction by Parasitic Oscillation

As shown in Figure 2-18, if the power MOSFET is connected in parallel without connecting a gate resistor, parasitic oscillation tends to occur. Due to parasitic oscillation, the gate-to-source voltage, V_{GS}, exceeds the maximum rated value, or the power MOSFET malfunctions and generates heat, which may result in the destruction of the power MOSFET.

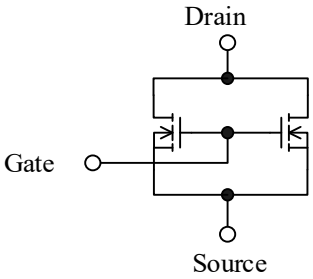


Figure 2-18. Connection in Parallel (no gate resistor)

● **Measures**

- The wiring should be as wide and short as possible to reduce the stray inductance.
- A resistor should be connected to the gate of each power MOSFET.
- Ferrite beads should be connected to the gate of each power MOSFET.

2.6.5. Destruction by ESD

The gate pin is sensitive to static electricity. If a static electricity or surge voltage generated by the human body or mounting equipment is applied to the gate and a static electricity capacitance of the gate is exceeded, the power MOSFET may be destroyed.

● **Measures**

- Connect the human body to the ground by a conductive strap or the like.
- Use conductive table mats on workbenches.
- Connect the equipment to the ground.

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