Development of Highly Efficient Controller of Synchronous Rectification for High-voltage Full-bridge LLC Power Supply

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Abstract In the recent development of LLC power supplies for large TVs and the high-voltage battery chargers of EVs, there has been demand for smaller transformers and the elimination, or at least the size and weight reduction, of heat sinks for power devices, to make the power supplies slimmer. As a solution to this requirement, the secondary side of the power supply is configured as a full bridge to achieve high output voltage and low current. Additionally, synchronous rectification has been used in order to further reduce the temperatures of power devices, and a new synchronous rectification controller IC has been developed for efficient switching control. In this paper, we report on the proprietary high-efficiency system that we have established.

1. Introduction

In recent years, TV screens have become larger and higher resolution, and in addition, the trend toward thinner screens has progressed dramatically, compared to a few years ago. For that reason, TV manufacturers are focusing on the development of slimmer technology for power supply boards.

The biggest obstacle in slimming down the power supply board is the thickness of the transformer and heat sink. To solve this obstacle, a full-bridge configuration of the secondary side of the LLC power supply was considered, to achieve higher output voltage and lower current. The windings on the secondary side of the transformer can be reduced and the transformer can be made smaller by using a high-voltage rectifier with a full-bridge configuration on the secondary side. In addition, synchronous rectification of the high-voltage rectifier and efficient switching control can lower the heat generation temperature of the power devices and eliminate the need for a heat sink. This paper reports on the development of a new synchronous rectification controller IC for efficient switching control.

2. Product Overview

This synchronous rectification IC, developed to slim down the power supply board, is intended for the full-bridge configuration of the secondary side of the LLC power supply, as shown in Figure 1.

The full-bridge configuration reduces the transformer secondary winding to half (one winding compared to two) at the same output power, compared to the center-tapped structure shown in Figure 2.

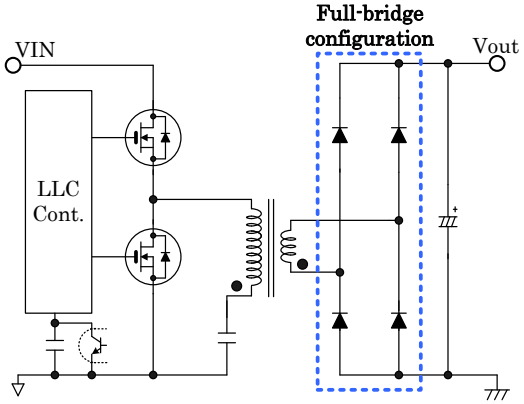

Figure 1: LLC Power Supply (Secondary Side Full-bridge Configuration)

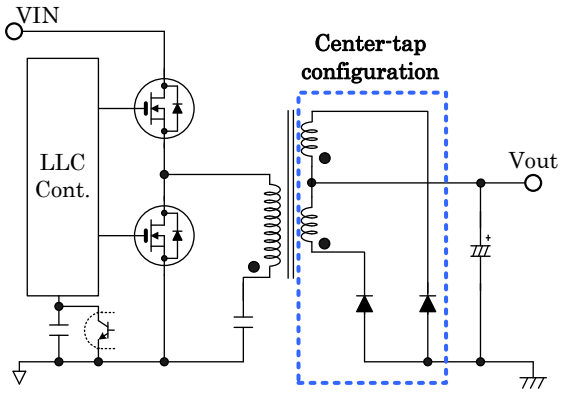

Figure 2: LLC Power Supply (Secondary Side Center-tapped Configuration)

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In addition, because there is no leakage inductance between the secondary windings and surge voltage generation is low, the voltage rating of the diodes can be less than half rectifier with a center-tap configuration. Therefore, there is no need to provide a voltage tolerance margin for the power device, compared to the center-tap configuration.

3. Secondary Side Synchronous Rectification Operation

To achieve synchronous rectification of the secondary side, the rectifier diode portion of the full bridge configuration on the secondary side in Figure 1 must be replaced with four power MOSFETs (hereinafter referred to as FETs) as shown in Figure 3, and the FETs must be driven with the timing shown in Figure 4. Q3 and Q4 on the low side shown in Figure 3 are main switches, while Q1 and Q2 on the high side are sub-switches. Efficient switching control of these four FETs reduces conduction losses and lowers the heat generation temperatures of the FETs.

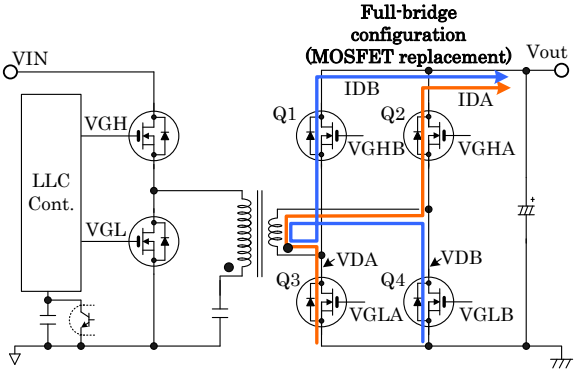

Figure 3: LLC Power Supply (Secondary side MOSFET Replacement)

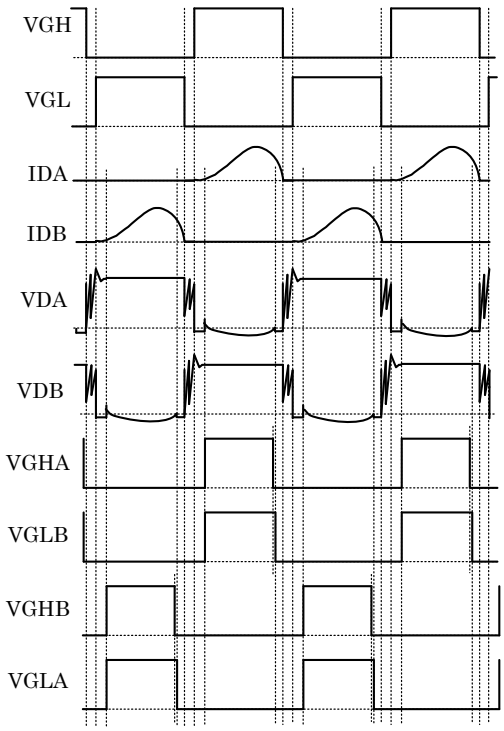

Figure 4: LLC Synchronous Rectification Operation Timing Chart

4. Control System

4.1. Block Structure of This Synchronous Rectification IC

Figure 5 shows a block diagram of this synchronous rectification IC. The voltage between the drain and source of Q3 and Q4 in Figure 3 is detected by VDA and VSA, and by VDB and VSB, as shown in Figure 6. This optimally controls the output timing of gate drive signals VGLA and VGLB for Q3 and Q4. Gate drive signals VGHA and VGHB for Q1 and Q2 are output in conjunction with VGLA and VGLB. A clock of several tens of MHz is used for internal control of the IC, and bit operations are performed at high speed based on information from one cycle earlier to control timing.

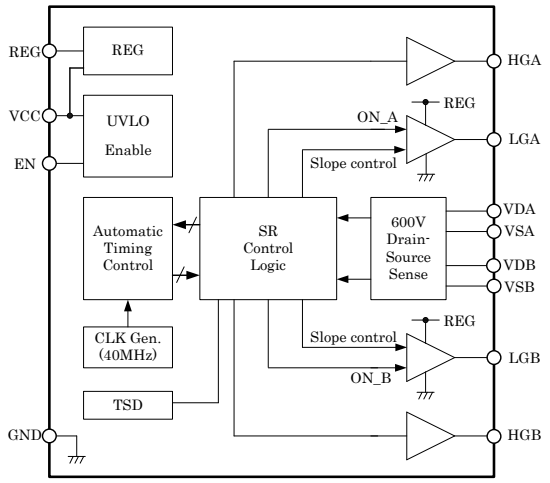

Figure 5: Block Diagram of This IC

4.2. Gate Drive Control of the Main Switches

The main switches, Q3 and Q4, perform digital drive control at the rising edge of the first half of the gate drive signal and slope control at the falling edge in the second half, as shown in Figure 6. In this IC, we have established and adopted a new driving method that combines both control types.

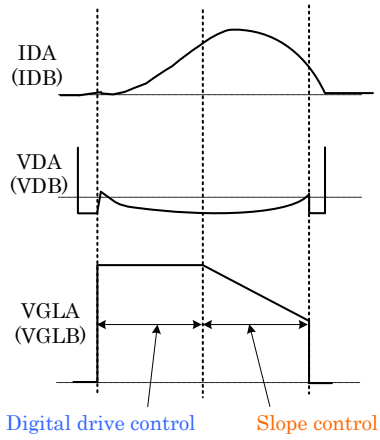

Figure 6 Gate Drive Waveform of This IC

In the case of digital drive control only, the switching speed of the gate drive signal can be increased and switching losses can be reduced. However, a large reverse voltage VL (hereinafter referred to as VL) is generated by the parasitic inductance of the FET leads shown in Figure 7 due to the sudden increase in the current change in I_{DA} (I_{DB}) just before turn-off time. This VL causes V_{DA} (or V_{DB}) to reach the off threshold early and the gate drive signal to turn off before I_{DA} at turn-off reaches 0A, as shown in Figure 8. This shortens the conduction period of the FET, which increases the conduction loss by the body diode and deteriorates efficiency.

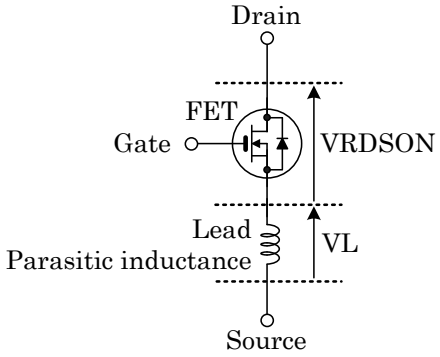

Figure 7: The Actual MOSFET

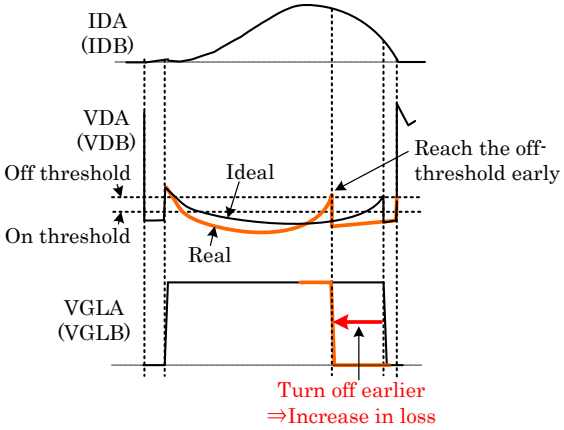

Figure 8: Ideal and Real Waveforms

To solve this problem, slope control was employed to control the on-resistance (R_{DSON}) by changing the slope of the gate drive signal during turn-off. Slope control detects the turn-off state of the gate drive signal one cycle earlier to determine the operation for the next cycle. When the gate drive signal is turned off early, the slope is controlled to be larger, and when it is turned off late, the slope is controlled to be smaller. Applying slope control to the gate drive signal prevents early turn-off by offsetting V_{RDSON}, ON voltage of FETs, and V_L induced by the parasitic inductor, shown in Figure 9. This can maximize performance as synchronous rectification.

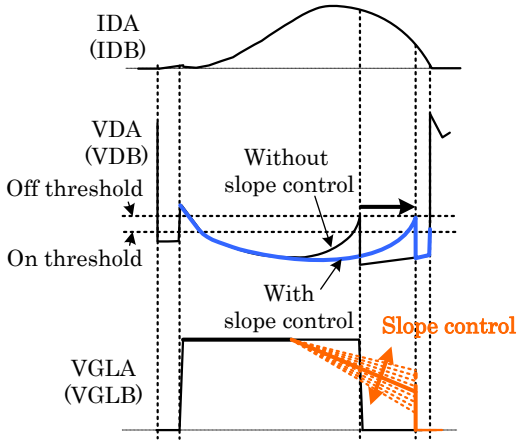

Figure 9: Effects of Slope Control

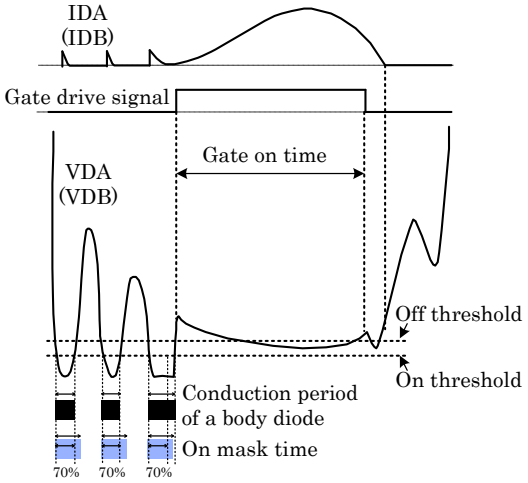

Figure 10: On-mask

4.3. On-mask Auto-adjustment Control

Ringing voltage is generated in the voltage waveform of the secondary winding when the channel of the conducting power device is switched. When the rectifier diode is replaced by an FET in synchronous rectification, the synchronous rectification IC detects that the voltage between the drain and source of the FET has reached the on threshold, and turns on the gate drive signal. For that reason, it is important to ensure that the IC controls the FETs not to malfunction due to ringing voltage.

In our previously developed synchronous rectification ICs, time setting to mask ringing voltage was done by an external pin. However, this has the disadvantage that the masking time is always the same even when the load changes, making it difficult to set the component constants [(1)]. In contrast, this IC determines the optimum on-mask time by counting the instances where the conduction time of the body diode immediately before gate turn-on, as shown in Figure 10, exceeds 70% of the on-mask time.

If the count is two or more times, the mask time for the next cycle is widened; if the count is less than two times, the mask time is narrowed. The gate drive signal turns on when the body diode conduction time is longer than the on-mask time.

This allows automatic adjustment of the mask time to obtain a gate drive signal with a wide conduction angle, thereby increasing efficiency.

5. Prototype Evaluation Results

5.1. Synchronous Rectification Operation

Figure 11 shows the operating waveforms of this synchronous rectification IC. During the period when the secondary winding current flows, the gate drive signal is optimally output by IC control.

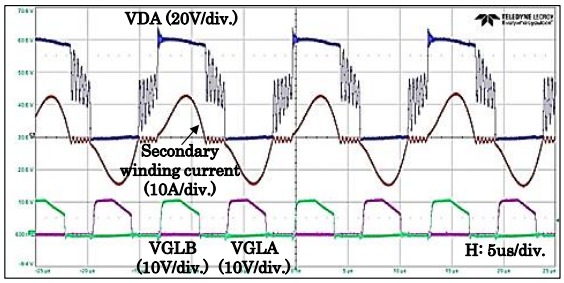

Figure 11: Synchronous Rectification Waveforms when at AC220V, Vo=60V, Io=6A Load

5.2. Characterization Results

Comparison of temperature and efficiency was made between center-tap diode rectification and synchronous rectification, using this IC in a full-bridge configuration at the same output power. The evaluation conditions are shown in Table 1.

Table 1: Evaluation Conditions

Configuration Control	Center tap Diode rectification	Full-bridge Synchronous rectification
Device	Diode	Power MOSFET
	200V/20A TO-220 10pcs (2ch/pc)	100V/8.6mΩ TO-220 4pcs
Heat-sink	120 × 50 × 7.5mm	None

Test model: 75-inch TV model board
Output power: 360W (VO=60V, IO=6A)
Aging: 2 hours

The evaluation results are shown in Table 2. In the case of diode rectification, 5 diodes (2 channel/pc) were used for each of Ach and Bch, and in the case of synchronous rectification, 2 FETs were used per channel (ch) (1 for H/S and 1 for L/S). The result is as follows, the synchronous rectification temperature averaged 54.6°C without a heat sink, demonstrating the favorable properties of synchronous rectification, on a par with diode rectification, which averaged 54.4°C with a heat sink. Good characteristics were also obtained in the efficiency and loss comparison in Figure 12.

Table 2: Evaluation Results

Configuration Control	Center tap Diode rectification			Full-bridge Synchronous rectification		
Transformer	72.0°C			70.2°C		
Heat-sink	120 × 50 × 7.5mm			None		
Device	Ach	#1	54.6°C	Ach	#1H/S	54.6°C
	Ach	#2	55.9°C		#2 L/S	55.6°C
	Ach/Bch	#3	54.0°C	Bch	#3 H/S	55.6°C
	Bch	#4	54.4°C		#4 L/S	54.6°C
	Bch	#5	53.2°C	-	-	-
	Average		54.4°C	Average		54.6°C

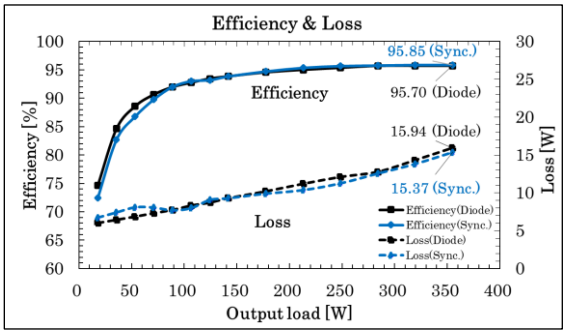

Figure 12: Efficiency and Loss Comparison

6. Conclusion

This IC was developed as a synchronous rectification IC for the secondary side of a high-voltage full-bridge LLC power supply. First, the voltage tolerance of the detection pins VDA and VDB is made high, which enables the output voltage to be high. Digital drive control and slope control were established as new gate drive controls. Prototype evaluation showed that even without a heat sink, the temperature was equivalent to that of a conventional diode configuration, and results showed that the area of the power supply board could be reduced. As a result of the above, the TV can be slimmed down by downsizing the transformer and eliminating the heat sink on the power supply board.

7. References

(1) Endo, Chikashige, LEE, Ito: Sanken Technical Report, Vol. 47, (2015.11)