NR130 Series
Application Note Rev.3.0

SANKEN ELECTRIC CO., LTD.

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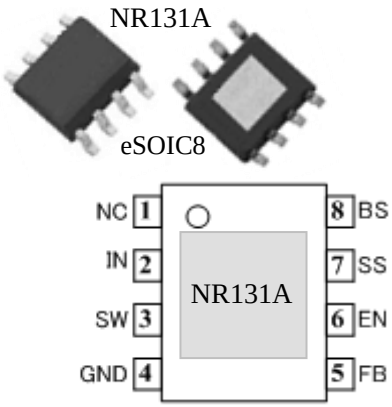
General Descriptions

The NR130 series is buck regulator ICs integrates High-side power MOSFETs. With the current mode control, ultra low ESR capacitors such as ceramic capacitors can be used. The ICs can realize super-high efficiency by performing pulse skip operation at light load condition. The ICs have protection functions such as Over-Current Protection (OCP), Under-Voltage Lockout (UVLO) and Thermal Shutdown (TSD). Soft starting time can be set up by selecting an external capacitor value. The ON/OFF pin (EN Pin) turns the regulator on or off and helps to achieve low power consumption requirements. The NR130 series is available in an 8-pin SOIC package with an exposed thermal pad on the back side and SOP8 package.

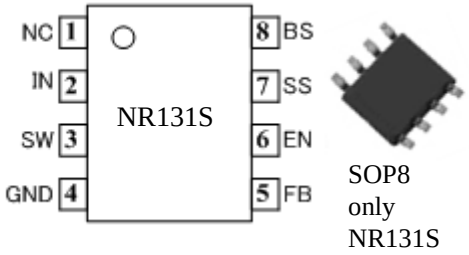
Features & Benefits

- Current mode PWM control
- Up to 94% efficiency at normal load condition
- Up to 85% efficiency at light load condition
- Stable with low ESR ceramic output capacitors
- Built-in protection function
  Over Current Protection (OCP)
  Thermal Shutdown (TSD)
  Under Voltage Lockout (UVLO)
- Built-in phase compensation
- Adjustable Soft-Start with an external capacitor
- Turn ON/OF the regulator function
- Programable Pulse-Skip operation

- Exposed SOIC 8 (NR131A)
  Thermally enhanced 8-Pin package



- SOP 8 (NR131S)



Electrical Characteristics

- 3A Continuous output current
- Operating input range V_{IN} = 4.5V～17V
- Output adjustable V_O = 0.8V～14V
- Fixed 350kHz frequency

Applications

- LCD TV / Blu-Ray / Set top box
- Green Electronic products
- Other power supply

Package

Series Lineup

Product No.	f_{SW}	V_{IN}		V_O		I_O	Pin 6 function	Package
NR131A	350kHz	4.5V to 17V	(1)	0.8V to 14V	(2)	3A	NC	Exposed SOIC 8
NR131S								SOP8

(1)The minimum input voltage shall be either of 4.5V or V_O+3V, whichever is higher.
(2) The I/O condition limited by the Minimum on-time ($T_{ON(MIN)}$) is in fig. 2.

1. Electrical Characteristics

1.1 Absolute Maximum Ratings

Table 1 Absolute maximum rating of NR130 series

Parameter		Symbol	Ratings	Units	Conditions
DC input voltage		V_{IN}	−0.3～19	V	
BS terminal voltage		V_{BS}	−0.3～25	V	
BS-SW Pin voltage		V_{BS-SW}	-0.3～6.0	V	DC
			−0.3～7.5	V	Pulse width≧30ns
SW terminal voltage		V_{SW}	−2～19	V	DC
			−4.5～19	V	Pulse width≧30ns
FB terminal voltage		V_{FB}	−0.3～5.5	V	
EN terminal voltage		V_{EN}	−0.3～19	V	
SS terminal voltage		V_{SS}	−0.3～7.4	V	
SS terminal allowable input current		I_{ssb}	5.0	mA	
Power dissipation (NR131A)	(3)	P_{D1}	1.76	W	Glass-epoxy board mounting in a 40×40mm. (copper area in a 25×25mm) Max T_J =150°C
Power dissipation (NR131S)	(3)	P_{D2}	1.42	W	Glass-epoxy board mounting in a 40×40mm. (copper area in a 25×25mm) Max T_J =150°C
Junction temperature	(4)	T_J	−40 ~ 150	°C	
Storage temperature		T_S	−40 ~ 150	°C	
Thermal resistance (junction- Pin No. 4)		θ_{JP1}	26	°C /W	(NR131A)
Thermal resistance (junction- Pin No. 4)		θ_{JP2}	60.8	°C /W	(NR131S)
Thermal resistance (junction-ambient air)		θ_{JA1}	71	°C /W	Glass-epoxy board mounting in a 40×40mm. (copper area in a 25×25mm) (NR131A)
Thermal resistance (junction-ambient air)		θ_{JA2}	88.2	°C /W	Glass-epoxy board mounting in a 40×40mm. (copper area in a 25×25mm) (NR131S)

(3) Limited by thermal shutdown.
(4) The temperature detection of thermal shutdown is about 165°C

1.2 Recommended Operating Conditions

Operating IC in recommended operating conditions is required for normal operating of circuit functions shown in Table 3 Electrical characteristics of NR130 series.

Table 2 Recommended operating conditions of NR130 series

Parameter		Symbol	Ratings		Units	Conditions
			MIN	MAX		
DC input voltage	(5)	V_{IN}	Vo+3	17	V	
DC output current	(6) (7)	I_O	0	3.0	A	
Output voltage		V_O	0.8	14	V	
Ambient operating temperature	(7)	T_{OP}	−40	85	℃	

(5) The minimum value of input voltage is taken as the larger one of either 4.5V or V_O +3V.
In the case of $V_{IN}=V_O+1 \sim V_O+3V$, it is set to I_O = Max. 2A

(6) A recommended circuit is shown in fig. 4.

(7) To be used within the allowable package power dissipation characteristics (fig. 5 , fig.6)

1.3 Electrical Characteristics

Electrical characteristics indicate specific limits, which are guaranteed when IC is operated under the measurement conditions shown in the circuit diagram (fig. 1)

Table 3 Electrical characteristics of NR130 series (Ta=25°C)

Parameter			Symbol	Ratings			Units	Test conditions
				MIN	TYP	MAX		
Reference voltage			V_{REF}	0.780	0.800	0.820	V	V_{IN} = 12V, I_O = 1.0A
Output voltage temperature coefficient			$\triangle V_{REF}/\triangle T$		±0.05		mV/°C	V_{IN} = 12V, I_O = 1.0A −40°C to +85°C
Switching frequency			f_{SW}	245	350	455	kHz	V_{IN}=12V, V_O=3.3V, I_O=1°
Line regulation		(8)	V_{Line}		10		mV	V_{IN} = 6.3V～18V, V_O = 3.3V, I_O = 1°
Load regulation		(8)	V_{Load}		70		mV	V_{IN} = 12V, V_O = 3.3V, I_O = 0.1°～3.0A
Over current protection threshold			I_S	3.1	4.5		A	V_{IN} = 12V, V_O = 3.3V
Supply Current(Non-switching)			I_{IN}		100		μA	V_{IN}= 12V, V_{EN}=12V
Shutdown Supply Current			$I_{IN(off)}$		1		μA	V_{IN}=12V, V_{EN}=0V
Input Under Voltage Lockout threshold			Vuvlo		3.9	4.4	V	V_{IN} Rising
SS Pin	Charging current		I_{SS}	13	22	31	μA	V_{SS}=0V, V_{IN}=12V
EN Pin	Sink current		I_{EN}		5	10	μA	V_{EN}= 12V
	Threshold voltage		V_{EN}	0.7	1.3	2.1	V	V_{IN}=12V
Max on-duty		(8)	D_{MAX}		90		%	V_{IN}=12V
Minimum on-time		(8)	$T_{ON(MIN)}$		170		nsec	V_{IN}=12V
Thermal shutdown threshold temperature		(8)	TSD	151	165		°C	V_{IN}=12V
Thermal shutdown restart hysteresis of temperature		(8)	TSD_hys		15		°C	V_{IN}=12V

(8) Guaranteed by design,not tested.

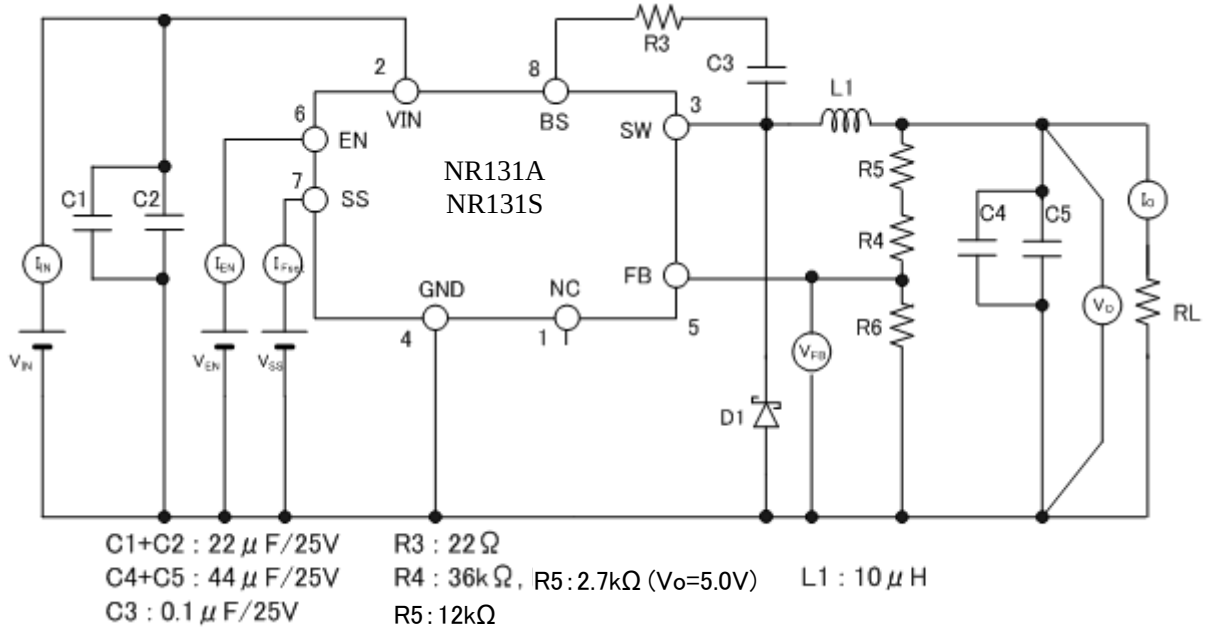


fig.1 Measurement circuit diagram

2. Block Diagram & Pin Functions

2.1 Functional Block Diagram

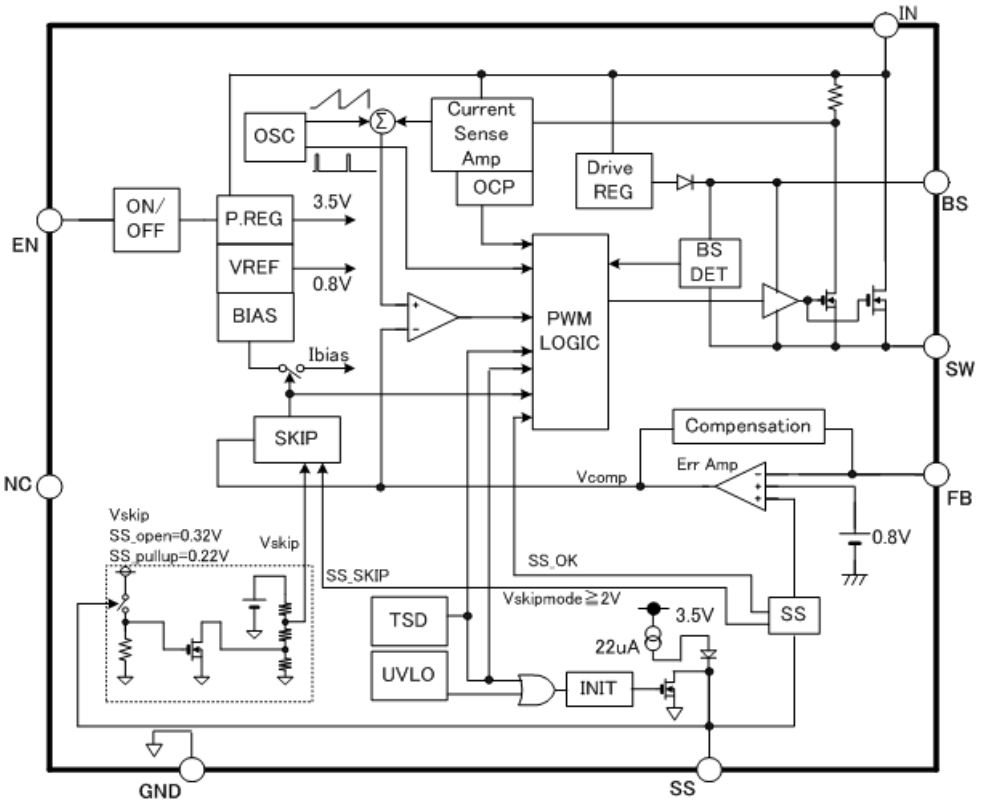


fig.2 Block diagram of NR131 series

2.2 Pin Asignments & Functions

fig.3 Pin Assignments

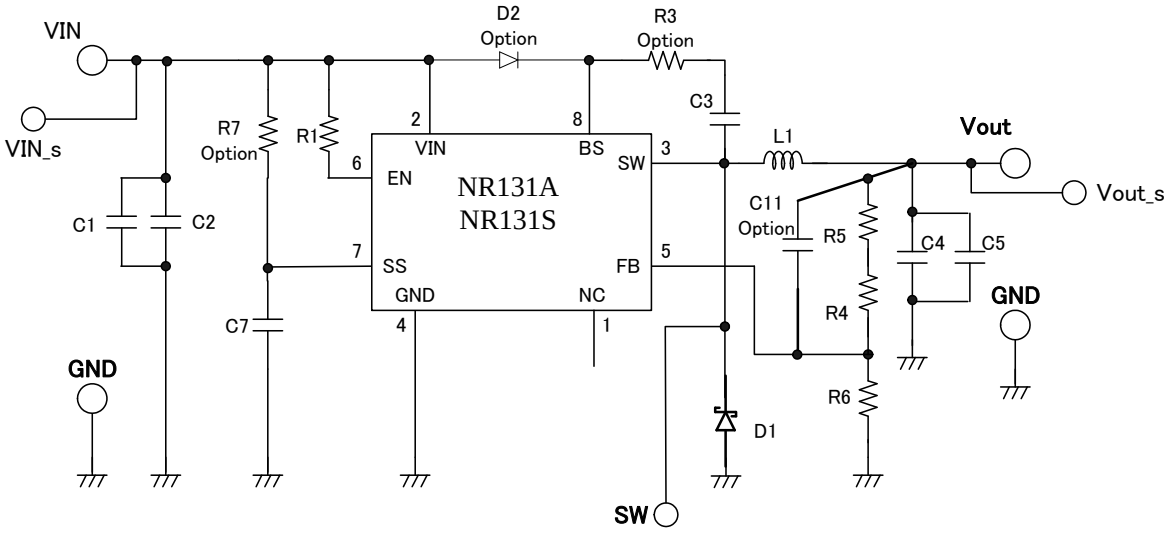
Table4 Pin assignments & functions of NR130A series

Pin No.	Symbol	Description
1	NC	No Connection.(NC)
2	IN	Power input. VIN supplies the power to the IC.as well as the regulator switches
3	SW	Power switching output. SW supplies power to the output. Connect the LC filter from SW to the output. Connect a Schottky Barrier Diode between SW and GND. Note that a capacitor is required from SW to BS to supply the power the High-side switch
4	GND	Ground Connect the exposed pad to Pin No.4(NR131A)
5	FB	Feedback input Pin to compare Reference Voltage. The feedback threshold is 0.8V. To set the output voltage, FB Pin is required to connect between resistive voltage divider R4 and R6.
6	EN	Enable input. Drive EN Pin high to turn on the regulator, low to turn it off.
7	SS	Soft-Start and SKIP operation control input. To set the soft-start period, connect to a capacitor between GND. To set the Low Ripple SKIP operation, add the resister 510k ohm between SS terminal and IN terminal.
8	BS	High-side Boost input. BS supplies the drive for High-side Nch-MOSFET switch. Connect a capacitor and a resistor between SW to BS.

3. Example Application Circuit

Each ground of all components is connected as close as possible to the Pin No.4 at one point.

To help heat dissipation, connect a large copper plane to exposed pad on the back side of the package. The copper plane is required for GND (NR131A).



C1, C2: 10µF / 25V	R1: 510kΩ	D1: SJPJ-L3
C4, C5: 22µF / 16V	R3: 10Ω	D2: Option
C3,C7: 0.1µF	R4: 36 kΩ, R5: 27kΩ (V_O=5.0V)	L1: 10µH
C11: 220pF(Option)	R6: 12kΩ, R7:510k Ω (Option)	

fig. 4 Typical Application Circuit of NR130 series

4. Allowable package power dissipation

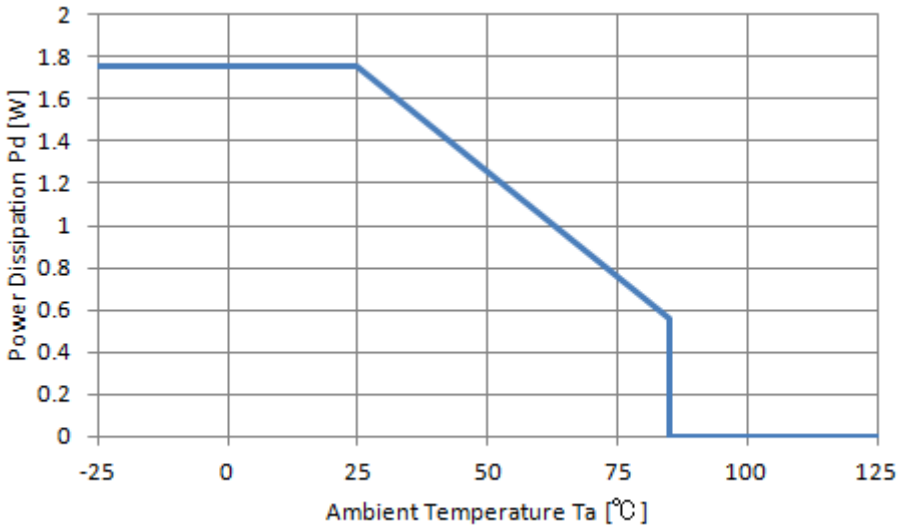


fig. 5 Allowable package powe disspation of NR131A

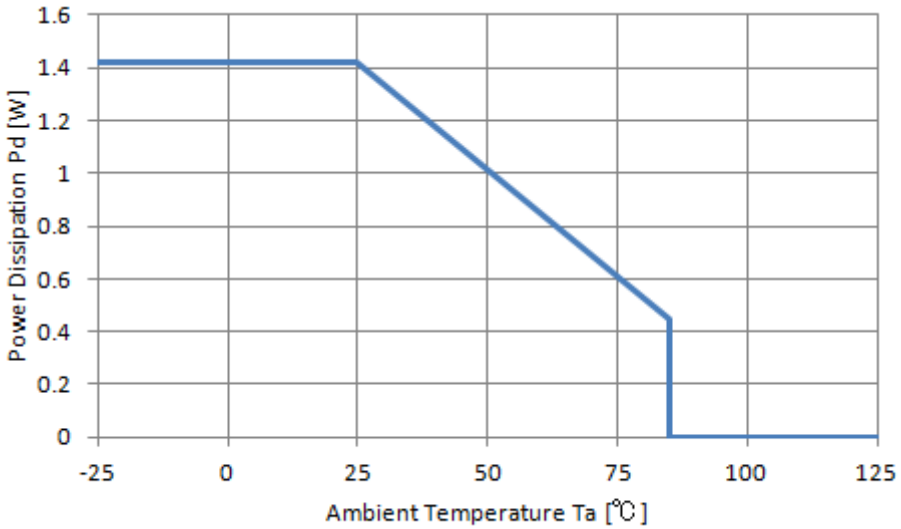


fig. 6 Allowable package powe disspation of NR131S

NOTES:

1) Glass-epoxy board mounting in a 30×30mm
2) copper area : 25×25mm
3) The power dissipation is calculated at the junction temperature 125 °C
4) Losses can be calculated by the following equation.
   As the efficiency is subject to the input voltage and output current, it shall be obtained from the efficiency curve and substituted in percent
5) Thermal design for D1 shall be made separately.

$$P_D = V_O \cdot I_O\left(\frac{100}{\eta x} - 1\right) - V_F \cdot I_O\left(1 - \frac{V_O}{V_{IN}}\right) \quad \cdots(1)$$

V_O: Output voltage

V_{IN}: Input voltage

I_O: Output current

η x: Efficiency(%)

V_F: Diode forward voltage
SJPJ-L3⋯0.45V(I_O=3A)

5. Package Outline

5.1.Exposed SOIC8 package (NR131A)

An outside size is supplied by either Package type A or Package type B.

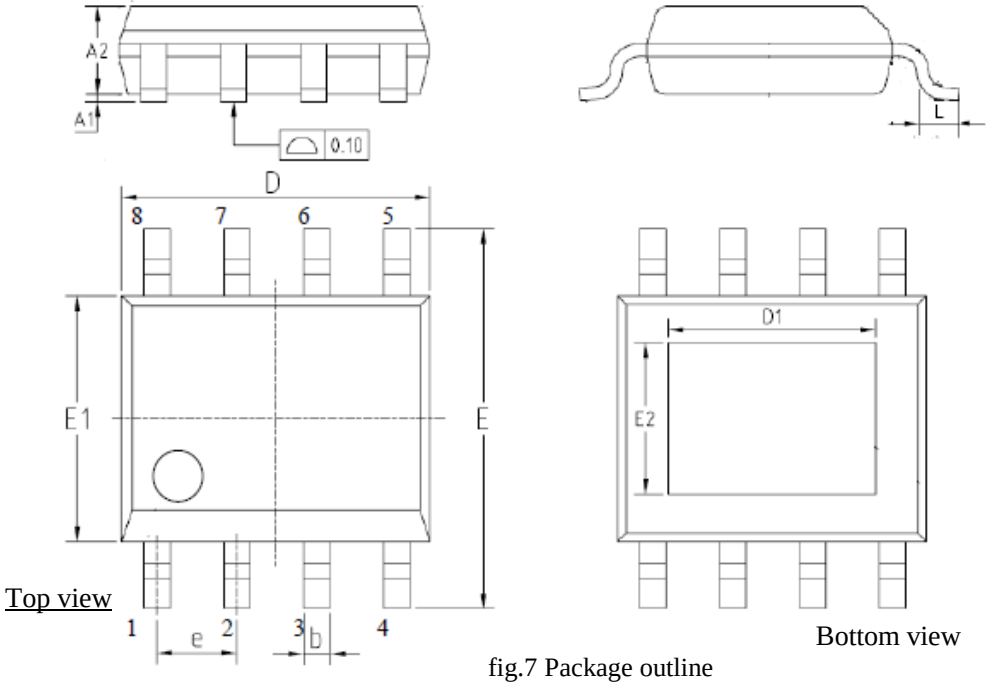


fig.7 Package outline

Symbol	Package A			Package B		
	MIN	TYP	MAX	MIN	TYP	MAX
A1	0	—	0.1524	0	0.10	0.15
A2	1.398	1.448	1.498	1.25	1.40	1.65
b	0.330	—	0.508	0.38	—	0.51
D	4.80	4.902	5.004	4.80	4.90	5.00
D1	3.053	3.18	3.307	3.10	3.30	3.50
E	5.893	—	6.918	5.80	6.00	6.20
E1	3.73	—	3.89	3.80	3.90	4.00
E2	2.033	2.16	2.287	2.20	2.40	2.60
e	—	1.27	—	—	1.27	—
L	0.508	—	0.762	0.45	0.60	0.80

Note:
1 Dimension is in millimeters.
2. Drawing is not to scale.

PIN Assignment
1.NC or COMP
2.IN
3.SW
4.GND
5.FB
6.EN
7.SS
8.BS

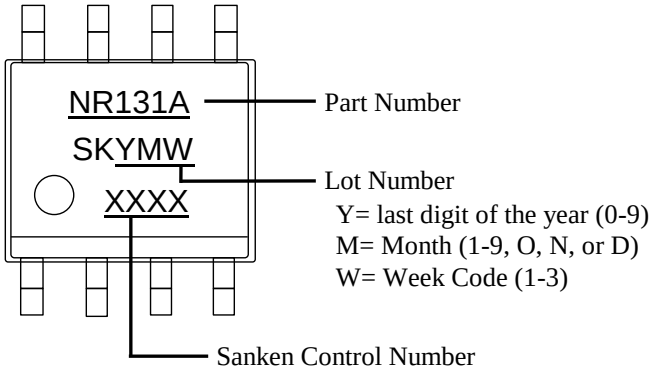


fig.8 Marking of NR130A series

5-2. SOP8 package（NR131S）

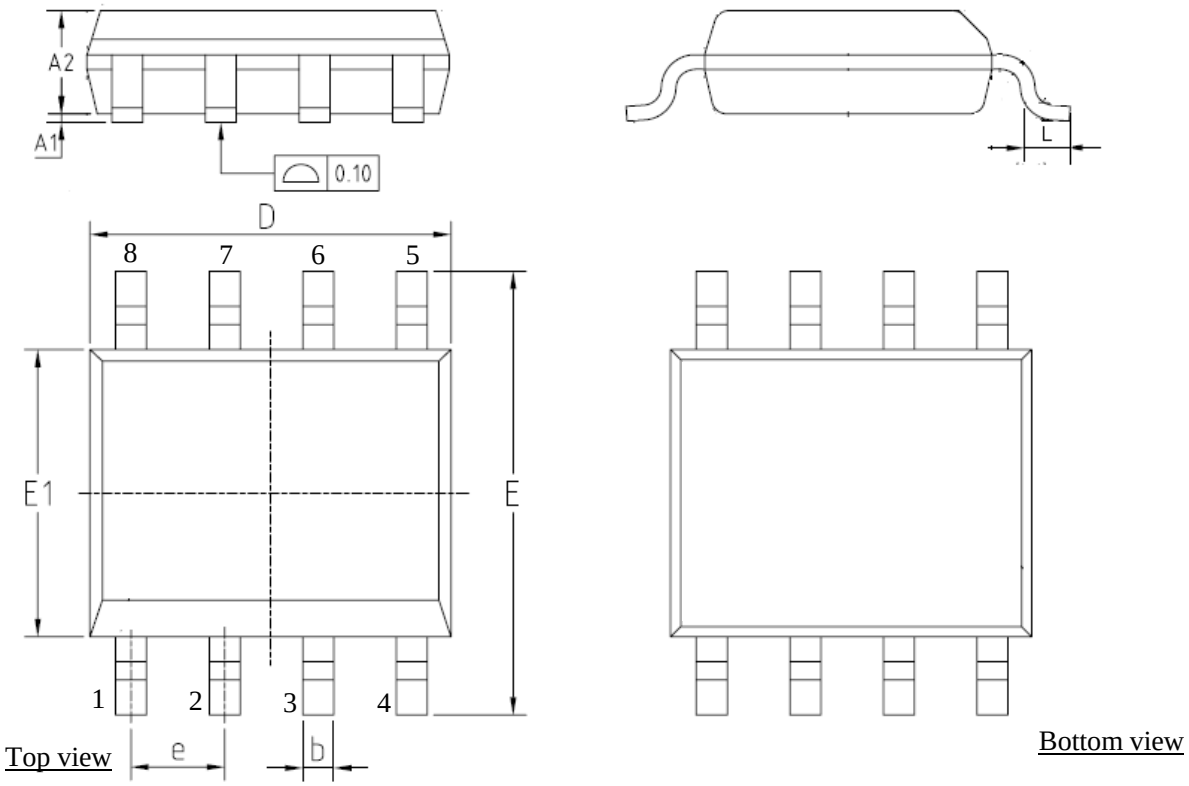
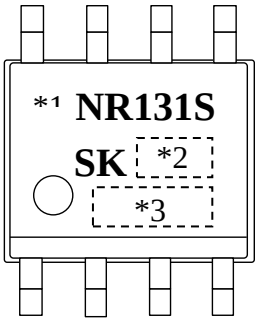


fig.9 Package outline and Marking of NR131S

*1. Product number

*2. Lot number (three digit)
1st letter : The last digit of the year
2nd letter : Month
January to September : 1 to 9
October : O
November : N
December : D
3rd letter : manufacturing week
First week to 5th week : 1 to 5
*3. Control number (four digit)



Symbol	Dimension is in millimeters(mm)		
	MIN	TYP	MAX
A1	0.05	0.15	0.25
A2	1.25	1.40	1.65
b	0.38	—	0.51
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	—	1.27	—
L	0.45	0.6	0.8

6. Operational Descriptions

The characteristic numerical value of the case without special mention writes TYP value according to the specifications of the NR130 series.

6.1 PWM (Pulse Width Modulation) Output Control

The PWM control circuit of NR130 series consists of error amplifier, a current sense amplifier, a PWM control comparator, and a slope compensation circuit. With error amplifier, the error amplification signal of the reference voltage 0.8V and FB terminal voltage is generated, and, on the other hand, the current detection signal proportional to the drain current of the switching transistor is generated with a current sense amplifier. In a PWM control comparator, when an error amplification signal is compared with a current detection signal and a current detection signal exceeds an error amplification signal, carrying out turn-off of the switching transistor performs PWM control. In addition, the current control signal is overlapped on the slope compensation signal, in order to avoid a subharmonic oscillation peculiar to current mode control.

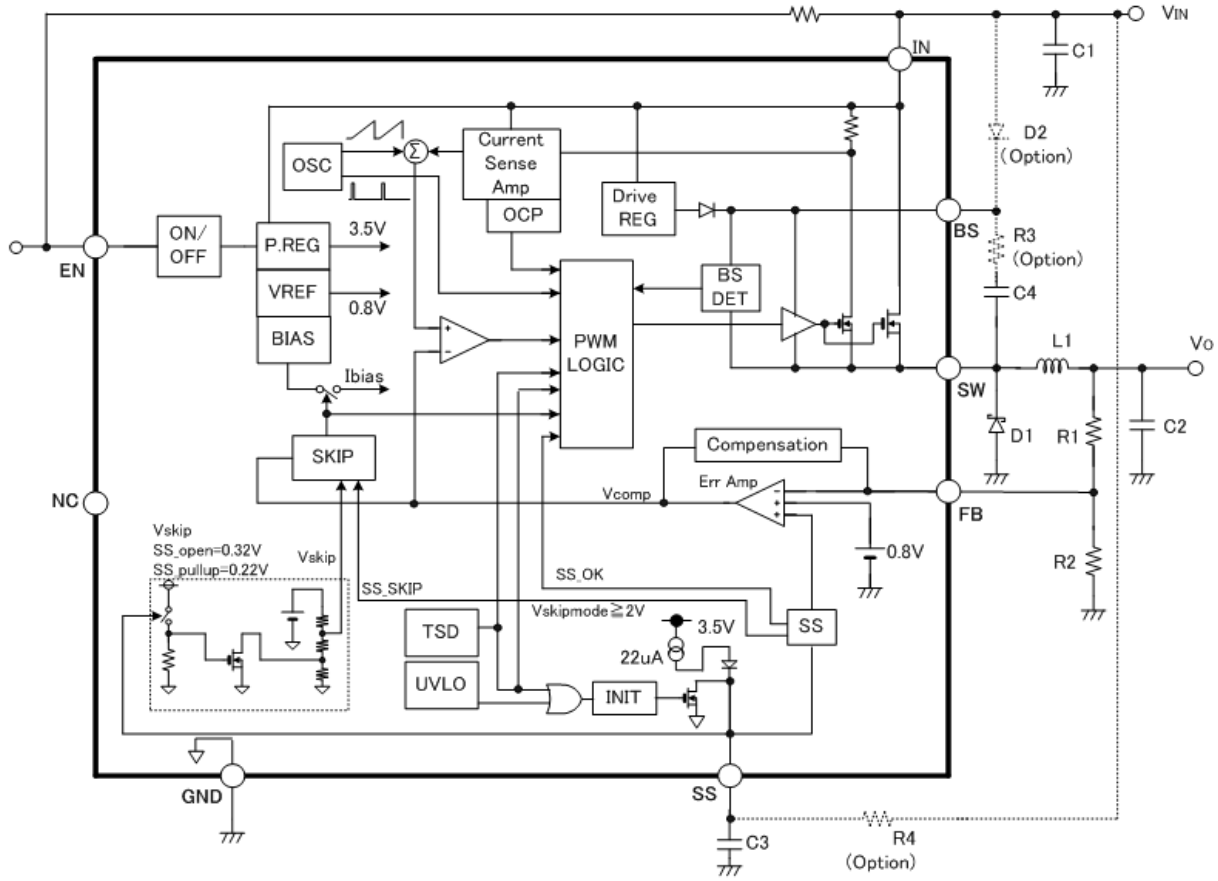


fig.10 Basic Structure of Chopper Type Regulator with PWM Control by Current Control

The NR130 series start the switching operation when UVLO is released, or EN or SS Pin voltage exceeds the threshold. Initially, it operates switching with minimum ON duty or maximum ON duty. The high-side switch (M1) is the switching MOSFET that supplies output power. At first, the boost capacitor C10 that drives M1 is charged by internal circuit. When M1 is ON, as the inductor current is increased by applying voltage to SW Pin and the inductor, the output of inductor current sense amplifier is also increased. Sum of the current sense amplifier output and slope compensation signal is compared with the error amplifier output. When the summed signal exceeds the error amplifier (Error Amp.) output voltage, the current comparator output becomes "High" and the RS flip-flop is reset. The regenerative current flows through D1, when the M1 turns OFF.

In NR130 series, the set signal is generated in each cycle and RS flip-flop is set. In the case that the summed signal does not exceed the error amplifier (Error Amp.) output voltage, RS flip-flop is reset without fail by the signal from OFF duty circuit.

6.2 Power Supply Stability

The stability of operation is decided by the acoustic phase coefficient of error amplifier, and the damping time constant of the low pass filter by the output capacitor C4 (C5) and the load resistance ROUT. In order to obtain stable operation. Please refer to "**7.1.3 Output Capacitor C4 (C5)**" and "**7.1.7 Output Voltage Set-up (FB Pin)**" .

6.3 Over Current Protection (OCP)

The NR130 series integrate the drooping type over-current protection circuit. The peak current of switching transistor is detected. When the peak current exceeds rated value, the over-current protection limits the current by forcibly shortening the ON time of transistor and decreasing the output voltage. It prevents the current increment at low output voltage by decreasing the switching frequency, if the output voltage drops lower. When the over-current state is released, the output voltage automatically returns.

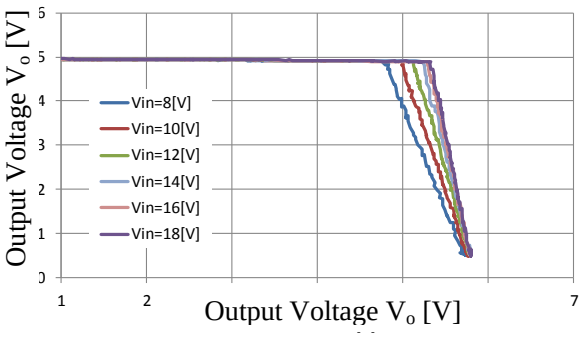


fig.11 OCP Characteristics of NR130 series

6.4 Thermal Shutdown (TSD)

The thermal shutdown circuit detects the IC junction temperature. When the junction temperature exceeds the rated value (around 165°C), it shuts-down the output transistor and turns the output OFF. If the junction temperature falls below the thermal shutdown rated value by around 15°C, the operation returns automatically.

* (Thermal Shutdown Characteristics) Notes

The circuit protects the IC against temporary heat generation. It does not guarantee the operation including reliabilities under the continuous heat generation conditions, such as short circuit for a long time.

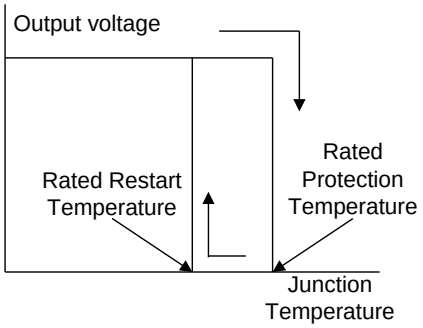


fig.12 TSD Characteristics of NR130A series

6.5 Soft-Start

By connecting a capacitor between Pin No.7 (SS) and Pin No.4 (GND), Soft-Start operates when the power is supplied to the IC. Output Voltage (Vo) is ramped up by the charge voltage level of Css.

Soft-Start time is denoted by the following formula.

(a) When R7 is not applied.

$$tss = Css \times (Vss2 - Vss1) / Iss \quad \cdots(2)$$

$$t\_delay = Css \times Vss1 / Iss \quad \cdots(3)$$

The SS terminal voltage which is connected to a capacitor for the software start , is rises by a internal constant current source.This is mostly raised as the fig13.

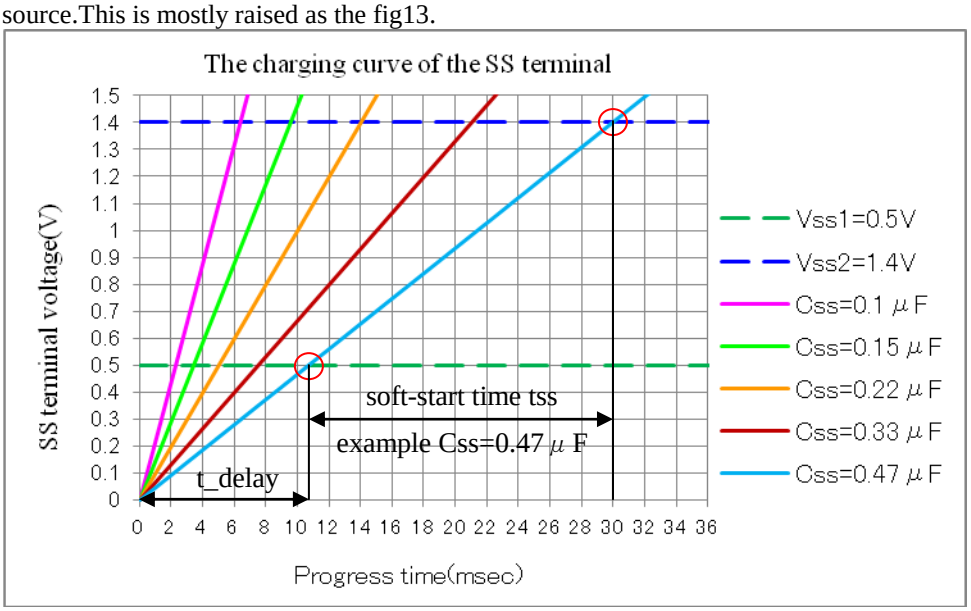


fig.13 Soft-start time without R7. (R7: Option resistor,for using pulse-skip-operation.)

After the input-voltage is supplied and EN-signal = “H”,～

The start delay time “t_delay”: The SS terminal-voltage is “0” ～ Vss1(=0.5V).

Vss1: (=0.5V, soft-start begin), Vss2: (=1.4V, soft-start finish)

While the SS terminal-voltage passes through Vss1 ～Vss2, It is soft-start time “tss”.

The time until an output voltage Vo rises up becomes t_delay+tss.(see fig15)

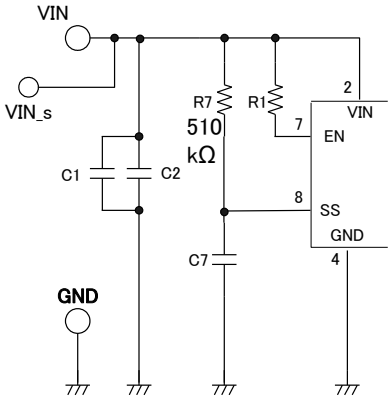


fig.14 Soft-Start circuit

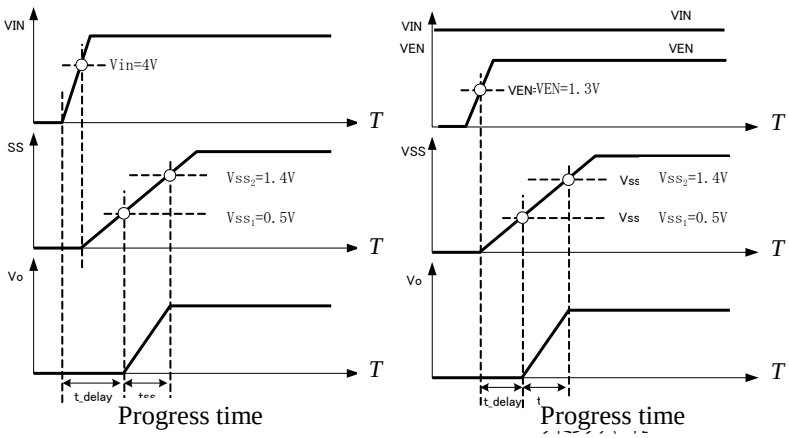


fig.15 Soft-Start operating description

(b) When R7 is applied.
* R7 is Option. Please refer to" **7.1.9.Pulse Skip mode change resistance R7**" for the application which uses R7. In this case, the current which charges Css becomes the total of current which passed through R7, and from the SS-terminal source. Adjust capacitance of Css referring to the fig16 because soft-start time is finishing early when therefore the Css is same capacitance.

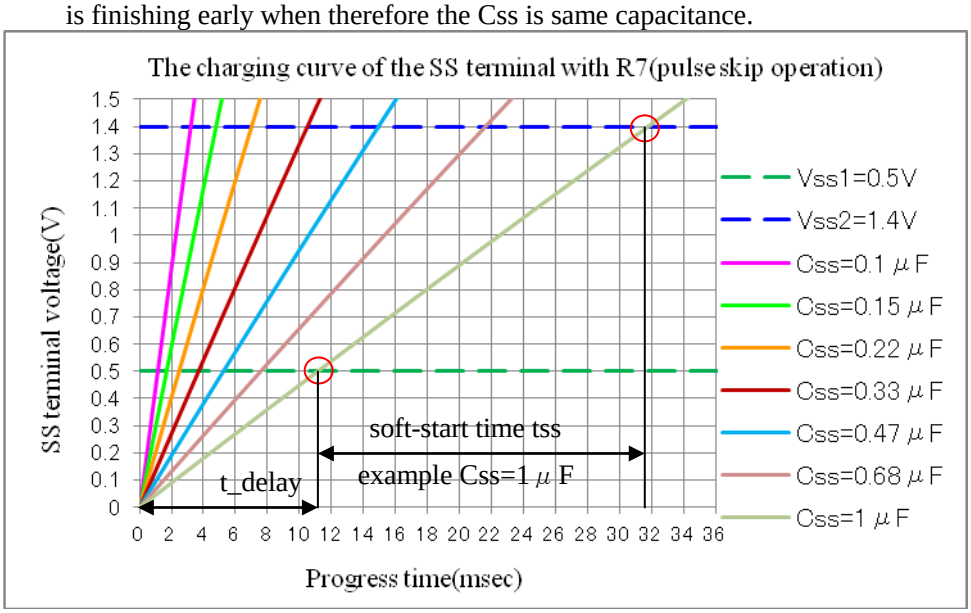


fig.16 soft-start time for using R7. (R7: Option resistor,for using pulse-skip-operation.)

When the current which passed through R7 is made Iss2, the SS terminal voltage at the time "t" is shown with the next equation.

$$Iss2 = \frac{VIN}{R7} \times e^{-\frac{t}{Css \times R7}} \quad \cdots(4) \qquad Vss(t) = \frac{(Iss + Iss2)t}{Css} \quad \cdots(5)$$

Iss=22μA(typ) : constant current

And, in the rise waveform of the output voltage Vo in the start-up , adjust the capacity of Css so that an excessive overshoot may not occur. This primarily occurs if tss is short. If soft start finishes before constant voltage control follows, waveform might become as shown in fig17. Take it into account that overshoot does not occur but start-up time also becomes longer as the capacity of Css increases.

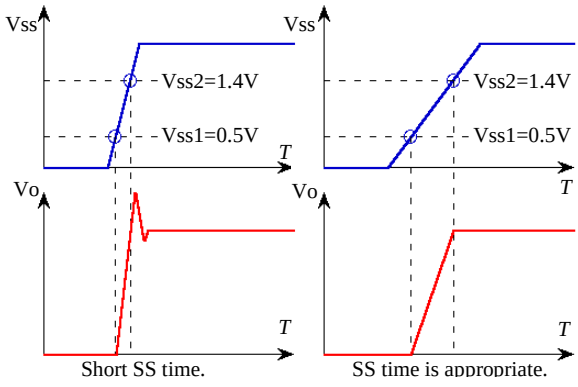


fig.17 image of Vo rise and overshoot .

About Css discharge to restart .

In such cases as “ON/OFF” operation with the EN-terminal, it is explained about the discharge of Css when this IC restarts.
Under the condition that charged-voltage is left in Css, when IC is restarted, in case of this IC, for a while, after SS-terminal-voltage is discharged to 0.5V by the compulsory discharge circuit, then the soft-start is resumed.(see fig18)
In case of the condition that charged-voltage is left in Css, after ON-signal is inputted, it takes the time of “t_discharge+tss” until Vo-waveform rise and stabilize. Well.
It thinks that the capacity of Css is decided after it confirms that over-shoot doesn’t occur in the waveform of rising output voltage.
As for the next,Confirm the time of “t_discharge+tss” in the Css capacity of the use.

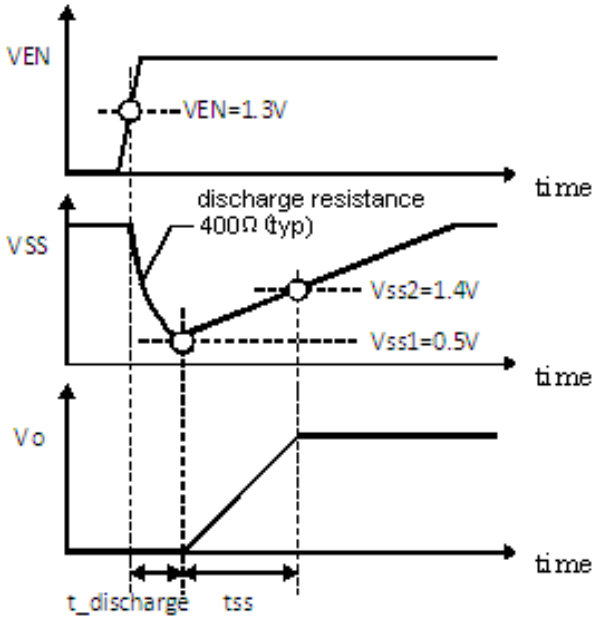


fig.18 Discharge time of SS capacitor

In case of the standard application(without pulse-skip setup resistor R7), and using setup resistor R7 for pulse-skip operation, the final charged-voltage “Vss (Full)” is different value.

*standard application (without R7)・・・Vss(Full)=2.8V(typ).
A clamp-voltage by the internal regulator’s voltage of this IC.
*Pulse-skip operation (use of R7 connected from Pin2 to Pin7) ・・・Vss(Full)=6.4V(typ).
A clamp-voltage by the internal protection element of this IC.

From this, the discharge time “t_discharge” of Css varies in the use condition.
As for the fig19 and fig20 are discharge-curve in case of Vss(Full)=2.8V and Vss(Full)=6.4V.

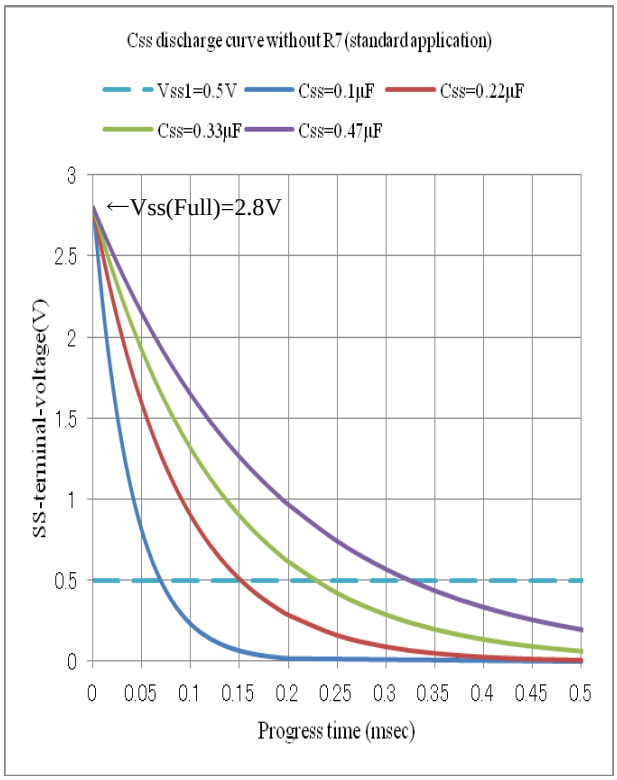


fig.19 Css discharge curve without R7
(standard application)

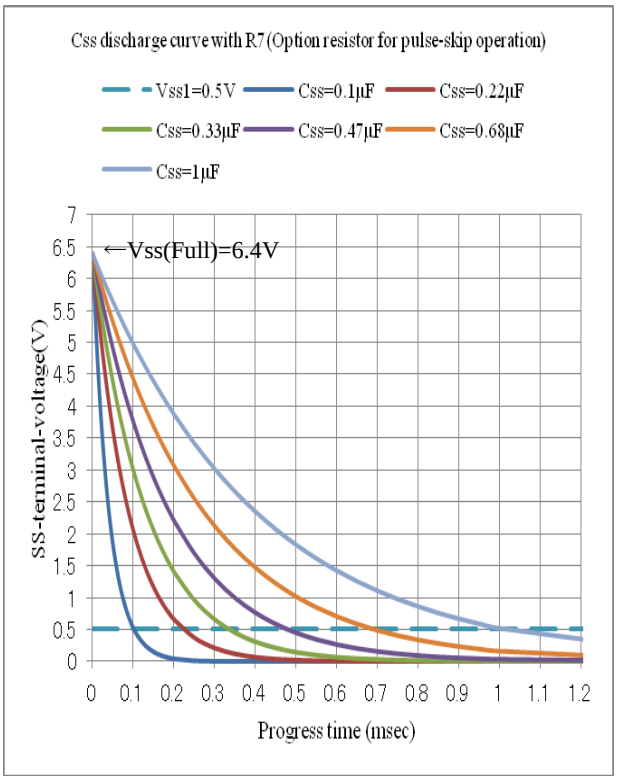


fig.20 Css discharge curve with R7
(Option resistor for palse-skip operation)

From the fig18,Css capacitor is discharged by discharge resistance of 400-ohm.
This discharge resistance is fixed inside the IC, and it can't be changed.
When the final charging voltage of Css is made Vss (Full), the discharge-voltage in the time "t" is found by the equation (6).

$$Vss(t) = Vss(Full) \times e^{-\frac{t}{Css \times 400}} \quad \cdots(6)$$

With an example of the fig19 and the fig20, until the SS-terminal-voltage discharges to 0.5V (=Vss1), though it is the short time of about 1 (msec) ,be careful of delay-time(= t_discharge) when there is the mode that "ON/ OFF" is operated repeatedly.

6.6 ON and OFF the Regulator (Enable)

EN Pin (Pin No.6) turns the regulator ON or OFF. When drive EN under 1.4V (V_{ENL}), output is turned OFF (fig21). 1.4V (V_{ENL}) can be achieved by connecting a bipolar transistor in an open collector configuration.
A UVLO threshold value is changeable by connecting resistance and adjusting the partial pressure ratio of resistance between IN-EN and between EN-GND.
(fig22)
Fig23 shows the correlation graph of the resistance between IN terminal and EN terminal, and a UVLO threshold value.

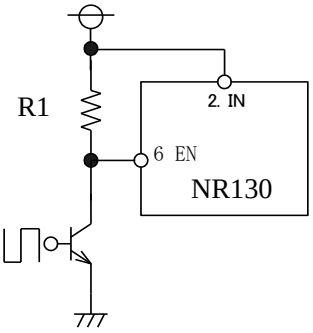


fig. 21 ON / OFF Control 1

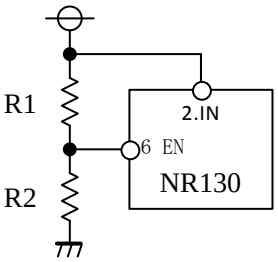


fig. 22 ON / OFF Control 2

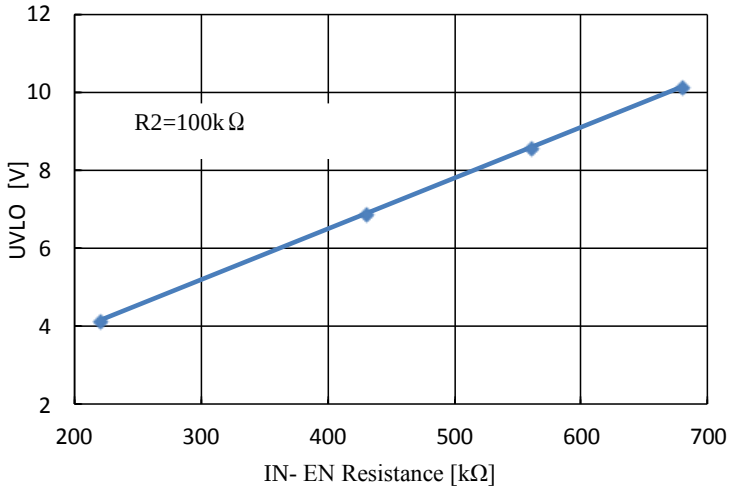
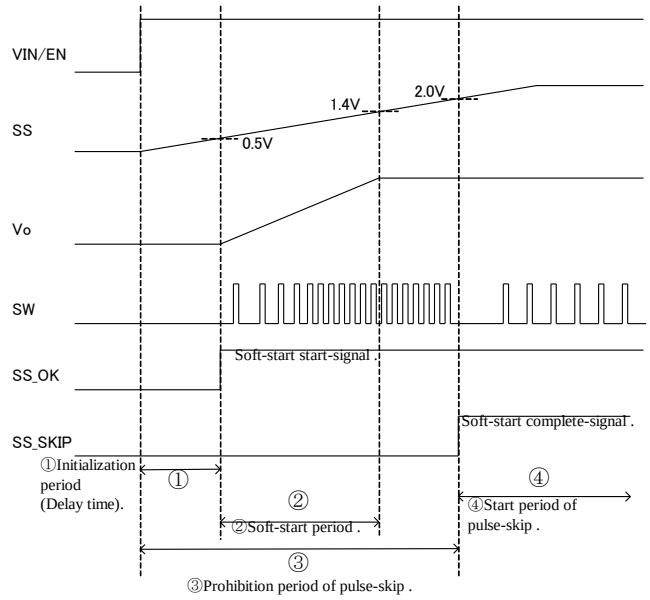


fig.23 ON or OFF threshold input voltage (UVLO)

*When "ON/OFF" by the outside signal isn't done, connect only R1 between the VIN～EN terminals, and use the resistance value of 470kΩ or 510kΩ.

6.7 About the pulse-skip mode in the light load condition

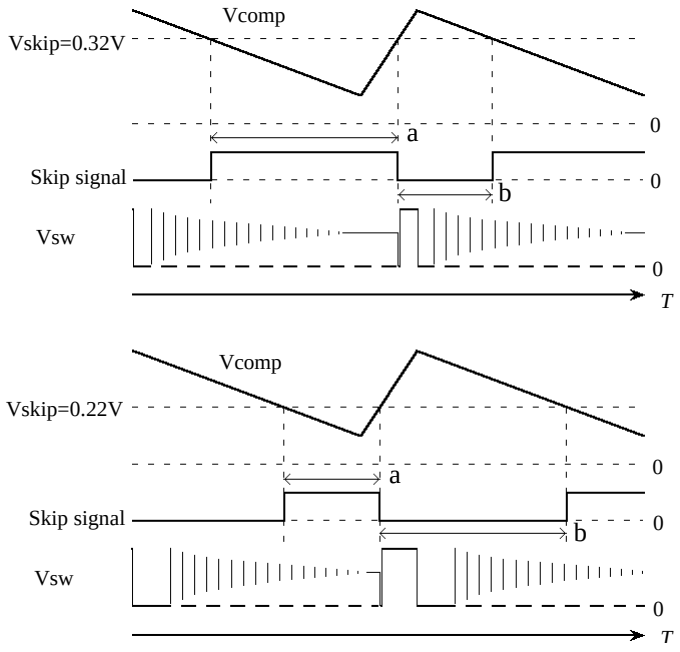
The pulse-skip-mode is built in the NR130 series with the standard to realize light load high efficiency.
Refer to the block diagram of the fig2.
As for the time of start up, by the SS terminal voltage, it is shifted from the pulse-skip-mode prohibition condition to a pulse-skip-mode prohibition release. By the resistor that is connected to the IN-terminal, it is possible to change the pulse-skip-mode range (Threshold).



1)About the transition of the start of the pulse-skip-mode.
i: A SS terminal starts a charging to SS-capasitor after the start-up. It is the initialization-period (Delay time) until the SS-terminal voltage rises to 0.5V .
ii: When the SS-terminal voltage reaches 0.5V, the start-signal of the soft-start (an internal signal) is outputted. The period when Vss rises from 0.5V to 1.4V, it becomes soft-start period. (The steady oscillation is done.).
iii: The pulse-skip-mode are prohibited until the SS-terminal voltage rises to 2.0V.
iv: After the complete-signal of soft-start is received when the SS-terminal voltage gets over 2.0V, the pulse-skip-mode becomes possible.

fig.24 The transition figure (*Startup of the IC. * Start-transition of the pulse-skip.)

2)About the range of the pulse-skip-mode(Threshold)
The threshold of the pulse-skip(Vskip) is compared with output(Vcomp) of the error-amplifier. And the skip-signal is formed. It becomes the pulse-skip movement by stopping the oscillation corresponding to that skip-signal.
i: When a SS terminal isn't connected to the IN terminal by the resistance, the threshold of the pulse-skip-mode(Vskip) is established in 0.32V, and the range of the pulse-skip-mode becomes wide.
ii: When a SS-terminal was connected to the IN-terminal by the resistor (510kΩ), the threshold of the pulse-skip-mode(Vskip) is established in 0.22V, and the range of the pulse-skip-mode becomes small.
In the fig25, about the setup resistor(510kΩ) which is between SS and VIN, the condition of the connection of the setup resistor is compared with the condition of the disconnection.



In the fig25, about the setup resistor(510kΩ) which is between SS and VIN, the condition of the connection of the setup resistor is compared with the condition of the disconnection.
VIN, Vo, the inductance of the inductor, the capacitance of the output capacitor and load-current Io and etc..., this is the case that other items are same conditions, and shows steady condition after the startup.
Vcomp is raised with the increase in load electric current.
When it exceeded the threshold of Vskip, the wave form of Vsw becomes the continuance of the steady oscillation mode(350kHz).
In the fig25, the wave-form of Vcomp is supposed the case that is the same condition persistently.
a: Off-period of pulse-skip oscillation
b: On-period of pulse-skip oscillation

fig.25 The comparative figure (*connection or disconnection of the setup resistor R7. *After the soft-start completed.).

Therefore, by the setup resistor of 510kΩ, and in case of Vskip=0.22V ,the load current that it shifts from the pulse-skip-mode to the continuous steady oscillation mode becomes small. And, in the fig25, during the pulse-skip (skip-signal= "H"), though the High-side switch is off .
As for the waveform of Vsw, because of the discontinuous inductor-current, ringing-wave form is formed, and this mostly converges to the output voltage Vo.
And, because the waveform of Vcomp varies according to the feedback condition of the constant voltage control,the period of the pulse-skip changes often, and the switching-pulse lasts from once to several times.

In the fig25, because of the internal circuit, you can't confirm the skip-signal directly from the outside of the package.

The resistor R7 (510kΩ) for the above pulse-skip setup : Refer to the explanation of '7.1.9 Pulse-skip mode change resistor R7' .
The capacitor C11 for the adjustment of the pulse-skip-waveform which contains the output ripple voltage waveform : Refer to the explanation of '7.1.8 Feedback Capacitor C11' .

7. Design Notes

7.1 External Components

All components are required for matching to the condition of use.

7.1.1 Choke Coil L1

The choke coil L1 is one of the most important components in the chopper type switching regulators. In order to maintain the stabilized regulator operation, the coil should be carefully selected so it must not enter saturation or over heat excessively at any conditions. The selection points of choke coil are as follows:

a)The coil type is only required for switching regulator

It is recommended not to use a coil for noise filer since it causes high heat generation due to high power dissipation.

b) Prevention of subharmonic oscillation

In the peak detection current control mode used by the NR130 series and so on, an inductor current's waveform might surge with a period of an integer multiple of the switching frequency under the condition in which control duty exceeds 0.5.

Such a phenomenon is called subharmonic oscillation, which is a problem caused in the peak detection current control mode in principle. In order to ensure stable operation, slope compensation is applied inside the IC. However, since only a fixed quantity of compensation is possible, it is necessary for even an application to select an appropriate inductor value corresponding to the output voltage. Concretely speaking, it is necessary to reduce the slope of the coil current.

The ripple portion of the inductor current, ΔIL, and the peak current, Ilp, are ontrolled from the following equations:

$$\Delta IL = \frac{(V_{IN} - V_O) \cdot V_O}{L \cdot V_{IN} \cdot f} \quad \cdots (7)$$

$$IL_p = \frac{\Delta IL}{2} + I_o \quad \cdots (8)$$

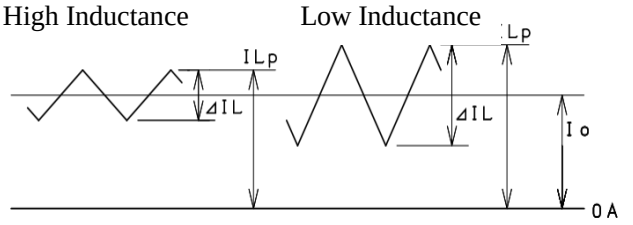


fig.26 Relationship between inductance and ripple current

According to the equations both ΔIL and Ilp increase as the inductance of the inductor, L, decreases.

Consequently, the inductor current becomes very steep if inductance is too small, so that the operation of the converter might become unstable. It is necessary to take care of an inductance decrease due to magnetic saturation such as in overload and load shortage. To prevent subharmonic oscillation, specify the condition of the slope of the inductor current by referring to Table 5.

Table 5 Specifying a slope of the coil current under a condition of Duty≧0.5 to prevent subharmonic oscillation.

VIN(V)	Vo(V)	Duty	Ton (μsec) Max	Slope of the inductor current K(A/μsec)	ΔIL(A)	Necessary inductance value (μH)Typ
17	14	0.82	3.360	0.134	0.450	22.40
17	12	0.71	2.880	0.260	0.749	19.24
17	10	0.59	2.400	0.436	1.046	16.06
15	12	0.80	3.264	0.156	0.509	19.24
12	9	0.75	3.060	0.208	0.636	14.43
10	7	0.70	2.856	0.267	0.763	11.24
9	6	0.67	2.720	0.312	0.849	9.62
9	5	0.56	2.267	0.499	1.131	8.02
8	5	0.63	2.550	0.374	0.954	8.02

* For Table 5, K is a specified value, so a value not more than K is recommended. For any values other than the ones combined in the table 5, begin to consider the values close to those ones.

*Duty=Vo/VIN･･･(9)、TonMax=Duty×(1／Fsw)･･･(10)、ΔIL=TonMax×K･･･(11)

$$L = \frac{(VIN - Vo) \times Vo}{\Delta IL \times VIN \times Fsw} \quad \cdots(12)$$ Fsw=Switching Frequency(Min)

* Combination under the condition of "VIN≧Vo+3V" in the specification.

c) Inductance calculation in the normal state

The inductance value of the coil under the condition of Duty < 0.5 is calculated using formula (12) mentioned above in the same way as applied under the condition of Duty≧0.5. However, for reference, Table 6 show the inductance values needed when ΔIL/Io = 0.2, which means the rate of ΔIL to the maximum load current, Io.

Table 6 Under a condition of Duty＜0.5("VIN≧Vo+3V" in the specification.)

VIN(V)	Vo(V)	Duty	Io(A)	Δ IL/Io(例)	Δ IL(A)	必要 L 値 (μ H)Typ
15	5	0.33	3	0.2	0.6	22.68
12	5	0.42	3	0.2	0.6	19.84
12	3.3	0.28	3	0.2	0.6	16.28
8	3.3	0.41	3	0.2	0.6	13.19
7	3.3	0.47	3	0.2	0.6	11.87
5	2	0.40	3	0.2	0.6	8.16
5	1.8	0.36	3	0.2	0.6	7.84
5	1.2	0.24	3	0.2	0.6	6.20

(About Table 6)

*ΔIL/Io can be specified freely. Setting 0.2 is consistently a setup example. Table 6 means that Io = 3A is the maximum load current.

*If the maximum load current Io is a small value such as 1.5A, if ΔIL/Io is set constant, the value of ΔIL becomes smaller, so that the needed inductance value becomes larger.

*When ΔIL/Io increases, inductance decreases. However, there is a matter of trade-off, for example, the output ripple voltage increases.When reducing ΔIL/Io, necessary inductance increases, and the external form of the coil becomes larger. Setting ΔIL/Io to 0.2 or 0.3 is conventionally regarded as a setting for good cost performance.

*When enlarging inductance, if the external form of the coil is identical, the coil turning increases and the winding-wire's diameter decreases. (→Direct current resistance"DCR"increases.)

*Direct current resistance"DCR"increases, too, so that it becomes impossible to make a large current flow. But,when giving priority to Low-DCR, the core size becomes larger.

* Select the most appropriate one in consideration of the conditions of use, mounting, heat dissipation, etc.

d) Confirm the DC superposition characteristics

The choke coil's inductance has the DC superposition characteristics by which inductance decreases gradually to the flowing DC current, depending on the material/shape of the core. Be sure to confirm if the inductance value is significantly lower than the design value when making the maximum load current for practical use flow. Obtain the data of the DC superposition characteristics including graphs from the manufacturer of the coil to understand the characteristics of the coil used in advance.

In doing so, important parameters are:

1) Saturation point...At what ampere does magnetic saturation occur?
2) Inductance fluctuation with the practical load current

* For example, since the product is used up to the condition of Io = 3A under practical load, using coils with a saturation point of 2A and so on are not allowed.
In addition, be careful with coils, for example, whose inductance is 10μH but this value becomes 5μH when a current of 1A flows.

e) Less noise

If the core is the open magnetic circuit type shaped like a drum, the magnetic flux passes outside the coil, so that the peripheral circuit might be damaged due to noise. Use a coil which has a core/structure of the low-leakage magnetic flux type. For details, consult the manufacturer of the coil.

f) Heat generation

In actuality, when using the coil for mounting the PCB, heat generation of the coil main body might be influenced by peripheral parts. In most cases, temperature rise of the coil includes the coil's own heat generation, and there are temperature restrictions such as below:

1) onboard(Cars) grade product: 150°C
2) highly-reliable product: 125°C
3) general product: 85-100°C

Be sure to evaluate heat generation because temperature rise differs when the PCB on which the coil is mounted is designed differently.
In general, coils with a smaller DCR value on the specification sheet have smaller loss.

7.1.2 Input Capacitor C1 (C2)

The input capacitor operates as a bypass capacitor of input circuit. It supplies the short current pulses to the regulator during switching and compensates the input voltage drop. It should be connected close to the regulator IC. Even if the rectifying capacitor of AC rectifier circuit is in input circuit, the input capacitor cannot be used as a rectifying capacitor unless it is connected near IC.

The selection points of C1 (C2) are as follows:
a) The capacitor should be of proper breakdown voltage rating
b) The capacitor should have sufficient allowable ripple current rating

If the input capacitor C1 (C2) is used under the conditions of excessive breakdown voltage or allowable ripple current, or without derating, the regulator may become unstable and the capacitor's lifetime may be greatly reduced. The selection of the capacitor C1 (C2) is required for the sufficient margins to the ripple current. The effective value of ripple current Irms that flows across the input capacitor is calculated from the equation (13):

$$Irms \approx 1.2 \times \frac{Vo}{Vin} \times Io \quad \cdots \quad (13)$$

In the case of V_{IN} = 20V, I_o = 3A, V_o = 5V,

$$Irms \approx 1.2 \times \frac{5}{20} \times 3 = 0.9A$$

The capacitor is required for the allowable ripple current of 0.9A or higher.

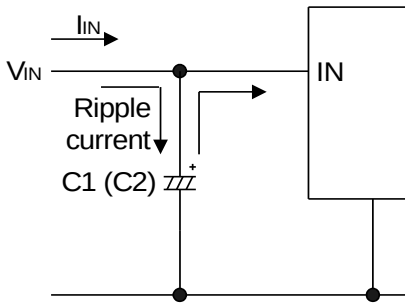


fig. 27 C1 (C2) Current path

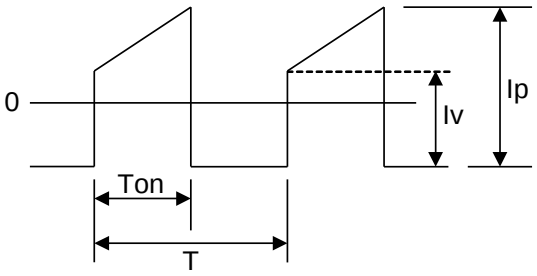


fig.28 C1 (C2) Current Waveform

7.1.3 Output Capacitor C4 (C5)

In the current control mode, the feedback loop which detects the inductor current is added to the voltage control mode. The stable operation is achieved by adding inductor current to the feedback loop without considering the effect of secondary delay factor of LC filter. It is possible to reduce the capacitance of LC filter that is needed to make compensations for the secondary delay, and the stable operation is achieved even by using the low ESR capacitor (ceramic capacitor).

The output capacitor C4 (C5) comprises the LC low-pass filter with choke coil L1 and works as the rectifying capacitor of switching output. The current equal to ripple portion ΔIL of choke coil current charges and discharges the output capacitor. In the same way as the input capacitor, the breakdown voltage and the allowable ripple current should be met with sufficient margins.

The ripple current effective value of output capacitor is calculated from the equation (14):

$$\mathrm{Irms} = \frac{\Delta \mathrm{IL}}{2\sqrt{3}} \cdots (14)$$

When ΔIL = 0.5A,

$$\mathrm{Irms} = \frac{0.5}{2\sqrt{3}} \fallingdotseq 0.14\mathrm{A}$$

Therefore a capacitor with the allowable ripple current of 0.14A or higher is needed.

The output ripple voltage of regulator Vrip is determined by the product of choke current ripple portion ΔIL (= C4 (C5) discharge and charge current) and output capacitor C4 (C5) equivalent series resistance ESR.

$$\mathrm{Vrip} = \Delta \mathrm{IL} \cdot \mathrm{C4_{ESR}} \cdots (15)$$

It is necessary to select a capacitor with low equivalent series resistance ESR in order to lower the output ripple voltage. As for general electrolytic capacitors of same product series, the ESR shall be lower for products of higher capacitance with same breakdown voltage, or of higher breakdown voltage with same capacitance.

When ΔIL = 0.5A, Vrip = 40mV,

$$\mathrm{C4_{ESR}} = 40 \div 0.5 = 80\mathrm{m\Omega}$$

A capacitor with ESR of 80mΩ or lower should be selected. Since the ESR varies with temperature and increases at low temperature, it is required to check the ESR at the actual operating temperatures. It is recommended to contact capacitor manufacturers for the ESR value since it is peculiar to every capacitor series.

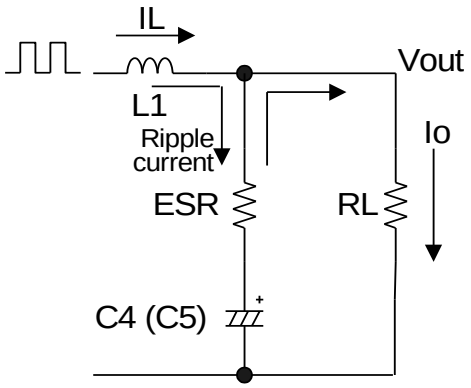


fig. 29 C4 (C5) Current path

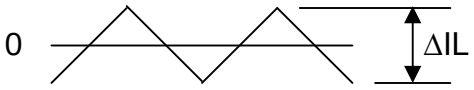


fig. 30 C4 (C5) Current Waveform

7.1.4 Output Voltage Set-up (FB Pin)

The FB Pin is the feedback detection Pin that controls the output voltage. It is recommended to connect close to the output capacitor C4 (C5). If they are not close, the abnormal oscillations may be caused by the poor regulation and the increased switching ripple.

The setting of output voltage is achieved by connecting between resistive voltage divider R4 (R5) and R6. Setting the I_{FB} to about 0.1mA is recommended.

(The target of I_{FB} lower limit is 50uA, and the upper limit is not defined. However, it is necessary to consider that the circuit current shall increase according to the I_{FB} value.)

R4 (R5), R6 and the output voltage are calculated from the following equations:

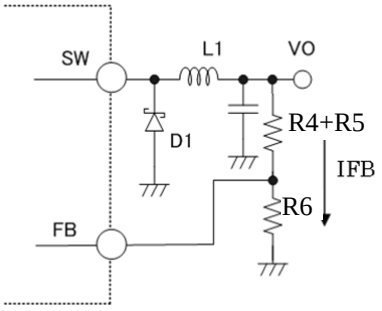


fig. 31 Detection and setting of output voltage

$I_{FB} = V_{FB} / R6$ ・・・(16) $*V_{FB} = 0.8V \pm 2.5\%$

$R4 + R5 = (V_O - VFB) / I_{FB}$ ・・・(17)

$R6 = V_{FB} / I_{FB}$ ・・・(18)

$V_O = (R4 + R5) \times (VFB / R6) + VFB$ ・・・(19)

R6 is required to connect for the stable operation when set to $V_O = 0.8V$.

Regarding the relation of input / output voltages, it is recommended that setting of the ON width of the SW Pin is more than 200nsec

The PCB circuit traces of FB Pin, R4 (R5) and R6 are required for not parallel to the flywheel diode. The switching noise may affect the detection voltage and the abnormal oscillation may be caused. Especially, it is recommended to design the circuit trace short from FB Pin to R6.

7.1.5 External Bootstrap Diode for Low Input

Although the NR13**0** series drives with input voltages lower than 6V, it is recommended to connect a diode between IN Pin and BS Pin in order to enhance the efficiency (fig.32). Alternatively an external voltage source can be connected through a diode to the BS Pin (fig.33).

NOTES:

1) The input voltage between BS and SW is required to be set less than 5.5V.

2) In the case that the input voltage V_{IN} is higher than 6V, the Bootstrap Diode must not be connected.

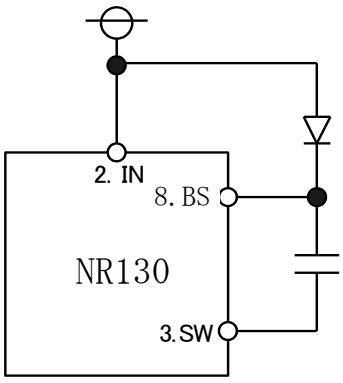


fig.32 Bootstrap Diode Connection 1

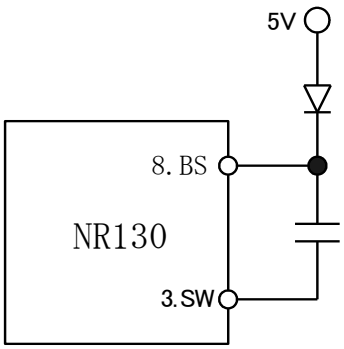


fig.33 Bootstrap Diode Connection 2

7.1.6 Flywheel Diode D1

A shcottky Barrier Diode as a flywheel diode is required for connection between SW Pin and GND.

The flywheel diode D1 is for releasing the energy stored in the choke coil at switching OFF. If a general rectifying diode or a fast recovery diode is used, the IC may fail to operate properly becase of applying reverse voltage due to the recovery and ON voltage. Since the output voltage from the SW Pin (Pin No. 3) is almost equal to the input voltage, it is required to use the flywheel diode with the reverse breakdown voltage of equal or higher than the input voltage.

It is recommended not to use ferrite beads for flywheel diode.

7.1.7 Output Voltage V_O and Output Capacitor C4 (C5)

From Table 7 shows the comparison of output voltage and output capacitor, for maintaining the IC stable operations, for reference.

ESR of Electrolytic Capacitor is required from 100m Ω to 200mΩ.

Regarding the inductance L, it is recommended to select it according to **7.1.1 Choke Coil L1**.

Table 7 V_O and C4 (C5) Comparison (NR131A/NR131D)

V_O(V)	C4 (C5) (μF)	
	Ceramic Capacitor	Electrolytic Capacitor (ESR≒100mΩ)
1.2	33 to 100	47 to 330
1.8	22 to 100	47 to 470
3.3	10 to 68	20 to 180
5	4.7 to 47	4.7 to 100
9	3.3 to 22	2.2 to 47
12	3.3 to 22	2.2 to 33
14	2.2 to 22	2.2 to 33

7.1.8 Feedback Capacitor C11

While carrying out pulse skip operation, large output ripple voltage may occur. The reason is for the number of times of a switch per 1-pulse skip cycle to increase by the delay of an error amplifire. As a measure, by adding the feedback capacitor C11, the number of times of a switch per 1-pulse skip can be reduced, and output ripple voltage can be controlled. Although there is no maximum of C11 value, since operation may become unstable when too large, please select in the range which is 100 pF ~470 pF.

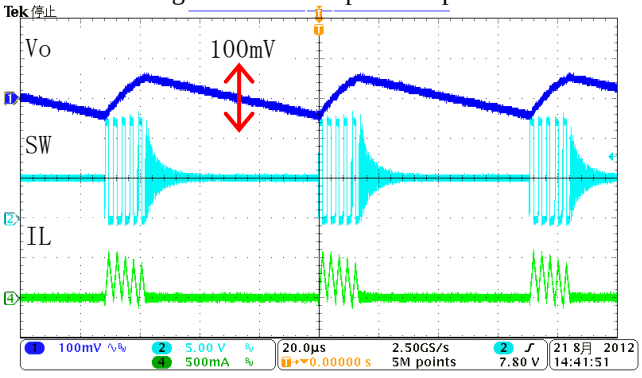


fig.34 The pulse skip waveform with large output ripple (C11=0pF)

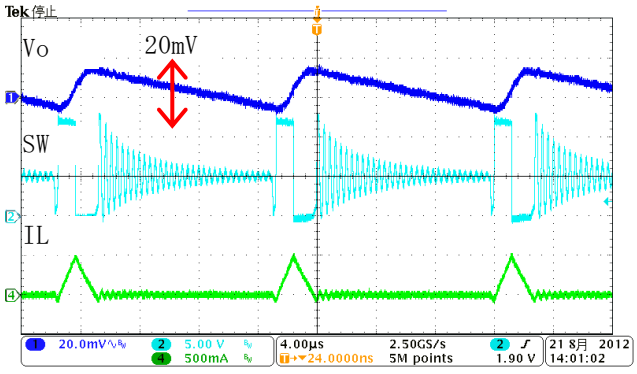


fig.35 The pulse skip waveform in ideal conditions (C11=220pF)

7.1.9 Pulse-skip mode change resistor R7

The relation between the Power MOS FET dorain peak current value (I_{DP}) in pulse-skip operation and average switching frequency (Fskip) shown in the following equation is.

$$Fskip \approx \frac{2 \cdot I_O \cdot (V_{IN} - V_O) \cdot V_O}{I_{DP}^{\ 2} \cdot L \cdot V_{IN}} \quad \cdots(20)$$

Since average switching frequency falls so that the drain peak current (I_{DP}) at the time of pulse skip operation is raised, light load efficiency improves, but on the other hand there is a tendency for output voltage Rippl to become large.

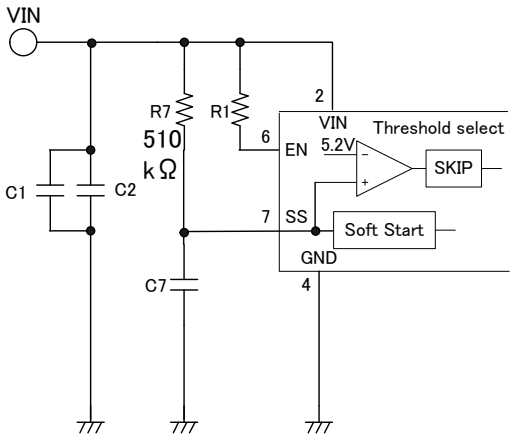


fig.36 The circuit condition at low ripple skip mode.

In order to solve this problem, This IC has a function which can choose average switching frequency and output ripple voltage in pulse-skip operation. In usual application, high level I_{DP} in pulse skip operation is selected and average switching frequency ontrolled very low. When output ripple voltage needs to be reduced still lower, Please add the resistance R7 (510kohm) between SS terminal and IN terminal. Since low level I_{DP} is chosen, output voltage Rippl becomes small.

Table 8 Relation between the R7 and pulse skip operational mode (Condition:VIN=12V,Vo=5V,L=10uH)

SS Pin condition	I_{DP}	Output Ripple	Frequency	Efficiency at light load
Without R7	600mAtyp	Small	Very low	Ultrahigh efficiency
With R7	100mAtyp	Very small	Low	High efficiency

*Though the resistance value of 510k-ohm is the E24 series,If acquisition is difficult with a supply problem,It can be substituted for 470k-ohm of the E12 series.

7.2 Pattern Design

7.2.1 High Current Line

High current paths in the circuit are marked as bold lines in the circuit diagram below. These paths are required for wide and short trace as possible.

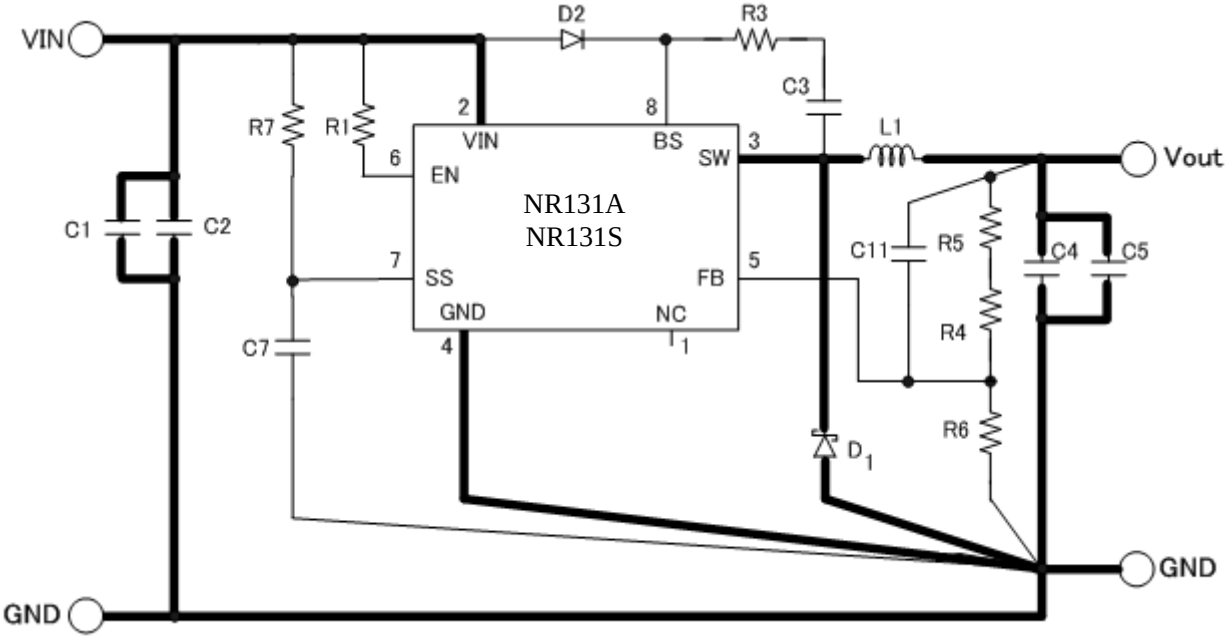


fig.37 Circuit Diagram

7.2.2 Input / Output Capacitors

The input capacitor C1 (C2) and the output capacitor C4 (C5) are required to connect to the IC as short as possible. If the rectifying capacitor for AC rectifier circuit is in the input side, it can be also used as an input capacitor. However, if it is not close to the IC, the input capacitor is required to be connected in addition to the rectifying capacitor. Since the high current is discharged and charged with high speed through the leads of input / output capacitors, make the current paths as short as possible. A similar care should be taken when designing pattern for other capacitors.

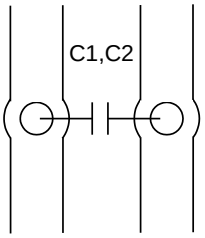


fig. 38 Recommended Pattern example

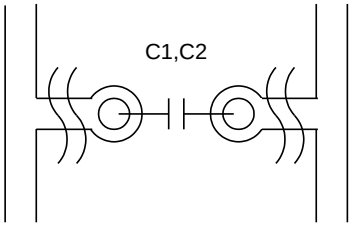
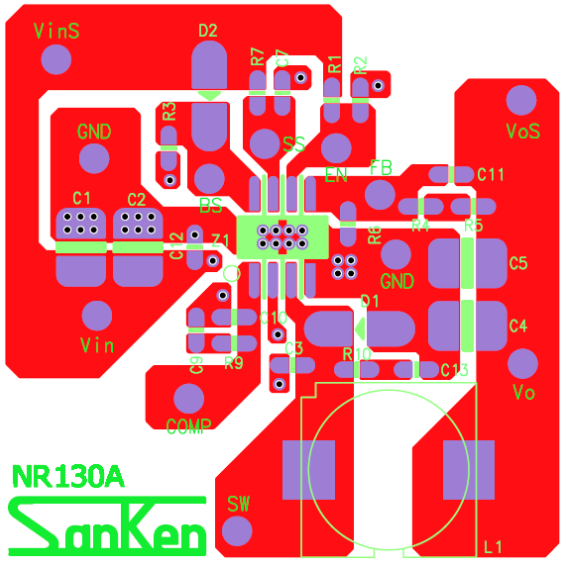


fig. 39 No good pattern example

7.2.3 The example of an Exposed SOIC8/SOP8 package mounting board pattern (NR131A/NR131S)



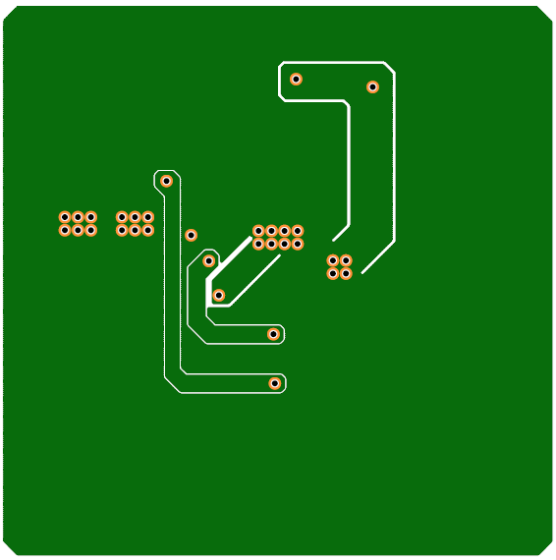
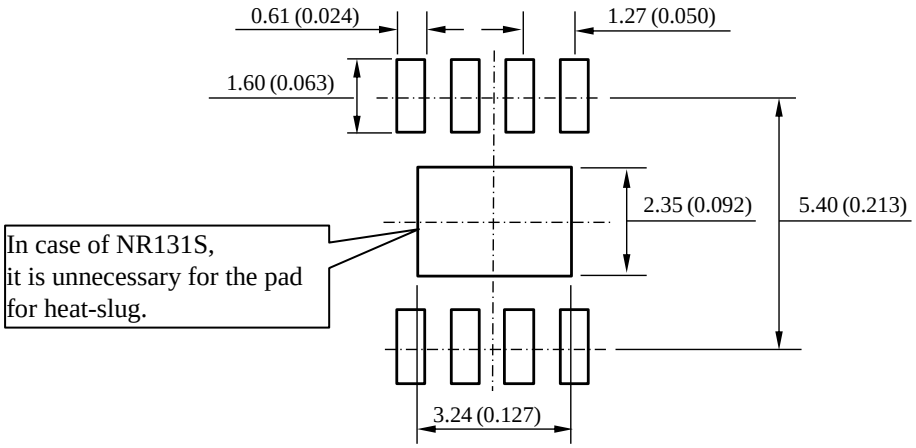


fig.40 Front Side: Component Side (double sided board) fig.41 Back Side: GND Side (double sided board)

*For the composition which contains an optional part, a part except for the standard circuit is arranged. Approve it.

NOTES:
Size of the PCB is about 60mm×60mm



NOTES:

1) Dimension is in millimeters, dimension in bracket is in inches.
2) Drawing is not to scale.

fig.42 Recommended land pattern

7.3 Applied Design

7.3.1 Spike Noise Reduction(1)

・The addition of the BS serial resistor

The "turn-on switching speed" of the internal Power-MOSFET can be slowed down by inserting R_{BS} (option) of the fig43.It is tendency that Spike noise becomes small by reducing theswitching-speed. Set up 22-ohm as an upper limit when you use R_{BS}.

*Attention

1) When the resistance value of R_{BS} is enlarged by mistake too much, the internal power-MOSFET becomes an under-drive, it may be damaged worst.
2) The "defective starting-up" is caused when the resistance value of R_{BS} is too big.
   *The BS serial resistor R_{BS} is R3 in the Demonstration Board.

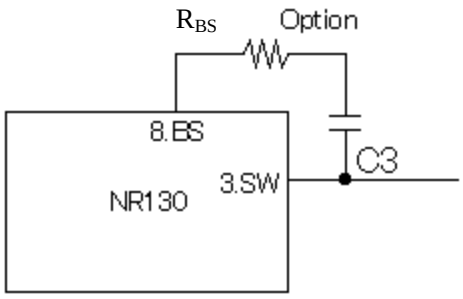


fig.43 The addition of the BS serial resistor

7.3.2 Spike Noise Reduction(2)

・The addition of the Snubber circuit

In order to reduce the spike noise, it is possible to compensate the output waveform and the recovery time of diode by connecting a capacitor and resistor parallel to the freewheel diode (snubber method). This method however may slightly reduce the efficiency.

* For observing the spike noise with an oscilloscope, the probe lead (GND) should be as short as possible and connected to the root of output capacitor. If the probe GND lead is too long, the lead may act like an antenna and the observed spike noise may be much higher and may not show the real values.

*The snubber circuit parts are C13 and R10.

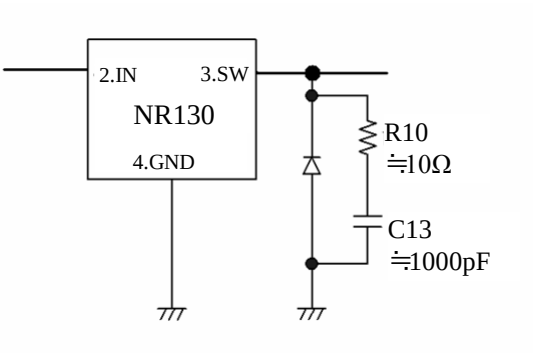


fig.44 The addition of the Snubber circuit

7.3.3 Attention about the insertion of the bead-core

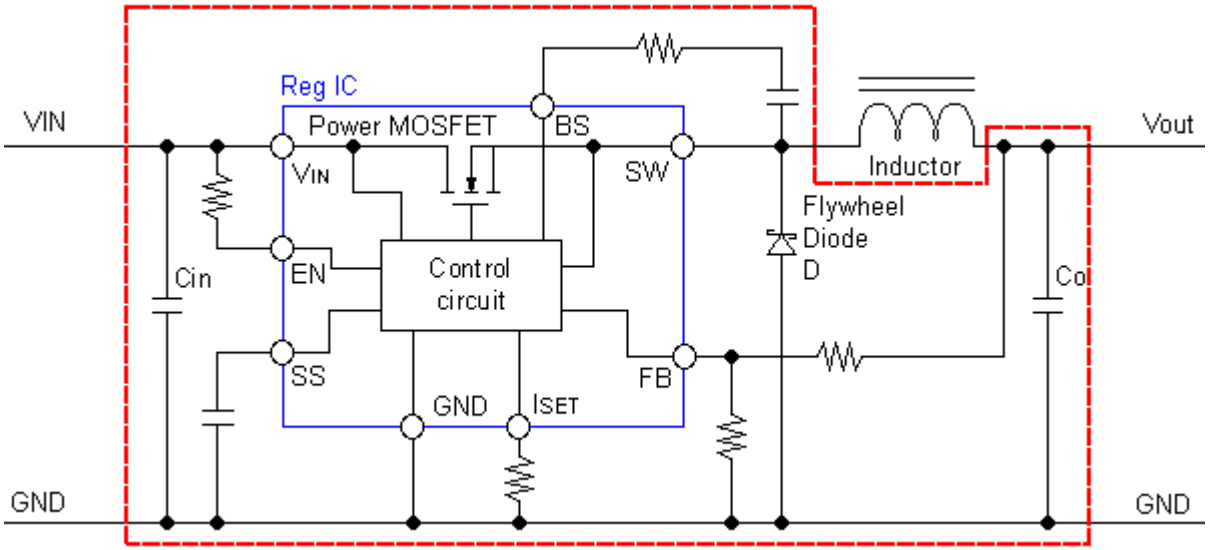


fig.45

In the area surrounded by the red dotted line within the fig45, don't insert the bead-core such as Ferrite-bead.
As for the pattern-design of printed-circuit-board, it is recommended that the parasitic-inductance of wiring-pattern is made small for the safety and the stability.
When bead-core was inserted, the inductance of the bead-core is added to parasitic-inductance of the wiring-pattern. By this influence, the surge-voltage occurs often, or , GND of IC becomes unstable, and also, negative voltage occurs often.

Because of this, faulty operation occurs in the IC. The IC has the possibility of damage in the worst case.
About the Noise-reduction, fundamentally, Cope by "The addition of CR snubber circuit" and "The addition of BS serial resistor".

7.3.4 Reverse Bias Protection

A diode for reverse bias protection may be required between input and output in case the output voltage is expected to be higher than the input Pin voltage (a common case in battery charger applications).

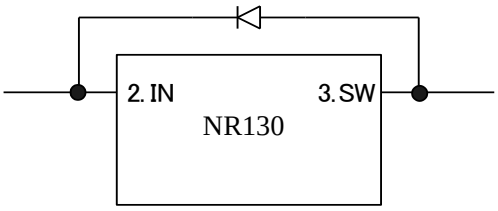


fig.46 Reverse bias protection diode

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