650 V, 30 A / 50A
3-phase Motor Drivers

SAM265Mx0AA1 Series

Data Sheet

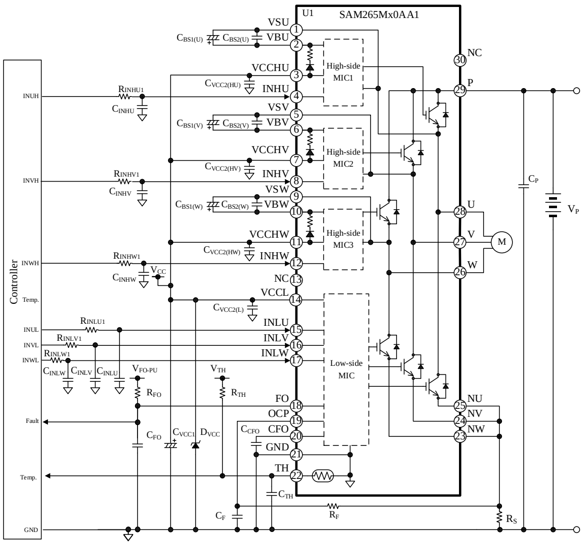
Description

The SAM265Mx0AA1 series are 3-phase brushless motor drivers in which output transistors, a pre-drive circuit, bootstrap diodes with current-limiting resistors, and a temperature-sensing thermistor are highly integrated. The ICs are suitable for driving 3-phase motor of an automotive high voltage auxiliary equipment system.

Features

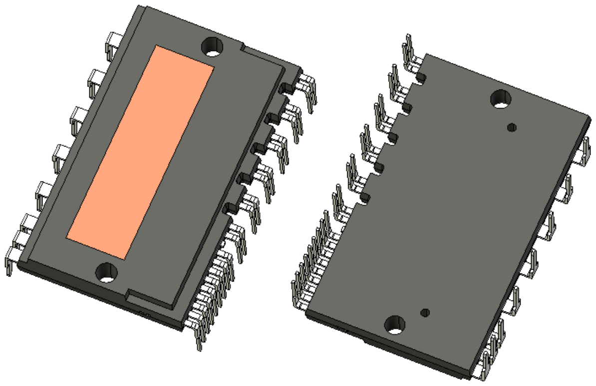
- AEC-Q100 Qualified
- Pb-free (RoHS Compliant)
- Isolation Voltage: 2500 V (for 1 min)
- Built-in Thermistor
- Built-in Bootstrap Diodes
- CMOS-compatible Input (3.3 V or 5 V)
- Fault Signal Output at Protection Activation
- Shutdown Signal Input
- Adjustable OCP Hold Time
- Protection Functions
  Undervoltage Lockout for Power Supply
    VBx Pin (UVLO_VBx): Auto-restart
    VCCL Pin (UVLO_VCCL): Auto-restart
  Overcurrent Protection (OCP): Auto-restart

Typical Application



Package

DIP30 (Leadform: 2540, 2541)



Not to scale
Not exactly match actual shape details

Selection Guide

Part Number	V_{CES}	Output Current
SAM265M30AA1	650 V	30 A
SAM265M50AA1	650 V	50 A

Applications

For driving 3-phase motor of the following high voltage auxiliary equipment system such as electrified vehicles (xEV):

- Electric Compressor
- Electric Oil Pump

Contents

1. Introduction

For pin descriptions, this docment employs a notation system that denotes a pin name with the arbitrary letter “x”, depending on context. The U-, V-, and W-phase (3-phases) output pins are represented as the pin numbers U, V, and W, respectively. Thus, “the VBx pin” is used when referring to any or all of the VBU, VBV, and VBW pins. When different pin names are mentioned as a pair (e.g., “the VBx and VSx pins”), they are meant to be the pins in the same phase. Also, “the OUTx pin” is used when referring to any or all of the output pins (U, V, and W).

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

2. Absolute Maximum Ratings

Unless specifically noted, T_A = 25 °C.

Parameter	Symbol	Conditions	Ratings	Unit	Remarks
Inverter Stage					
Main Supply Voltage (DC)	$V_{P(DC)}$	P–Nx	500	V	
Main Supply Voltage (Surge)	$V_{P(SURGE)}$	P–Nx	550	V	
Collector-to-Emitter Voltage (Surge)	$V_{CE(SURGE)}$	P–OUTx, OUTx–Nx	550	V	
Collector-to-Emitter Voltage	V_{CES}	Built-in IGBT chip	650	V	
Collector Current[1]	I_C	T_C = 25 °C	30	A	SAM265M30AA1
			50		SAM265M50AA1
Collector Current (Peak)	I_{CP}	T_C = 25 °C, pulse width < 1 ms, duty cycle < 1%	60	A	SAM265M30AA1
			100		SAM265M50AA1
Power Dissipation	P_C	T_C = 25 °C, 1 element operating (IGBT)	86.2	W	SAM265M30AA1
			125		SAM265M50AA1
		T_C = 25 °C, 1 element operating (freewheeling diode)	41	W	SAM265M30AA1
			54		SAM265M50AA1
Control Parts					
Nx Pin Voltage	V_{Nx}	Nx–GND	−5 to 5	V	
VCCHx Pin Voltage	V_{VCCHx}	VCCHx–GND	−0.5 to 25	V	
VCCL Pin Voltage	V_{VCCL}	VCCL–GND	−0.5 to 25	V	
VBx–VSx Pin Voltage	$V_{VBx\text{-}VSx}$	VBx–VSx	−0.5 to 25	V	
INHx Pin Voltage	V_{INHx}	INHx–GND	−0.5 to V_{VCCHx} + 0.3	V	
INLx Pin Voltage	V_{INLx}	INLx–GND	−0.5 to V_{VCCL} + 0.3	V	
FO Pin Voltage	V_{FO}	FO–GND	−0.5 to V_{VCCL} + 0.3	V	
FO Pin Sink Current	I_{FO}		1	mA	
OCP Pin Voltage	V_{OCP}	OCP–GND	−0.5 to V_{VCCL} + 0.3	V	
Change Rate of VCC Supply Voltage Time	$\Delta V_{VCC}/\Delta t$		−1 to 1	V/μs	

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[1] Should be derated depending on an actual case temperature.

Parameter	Symbol	Conditions	Ratings	Unit	Remarks
Bootstrap Circuit					
Bootstrap Diode Reverse Voltage	$V_{R\text{-}BS}$		650	V	
Thermistor					
Operating Thermistor Temperature	T_{TH}		−40 to 150	°C	
Thermistor Allowable Current	$I_{TH\text{-}MAX}$		1.8	mA	
Thermistor Allowable Power	$P_{TH\text{-}MAX}$		200	mW	
Common					
Junction Temperature[2]	T_J		−40 to 150	°C	
Operating Case Temperature[3]	T_C	For the measurement point, see Figure 2-1 or Figure 2-2.	−40 to 125	°C	
Storage Temperature	T_{STG}		−40 to 150	°C	
Isolation Voltage[4]	$V_{ISO(RMS)}$	Between surface of heatsink side and each pin; AC, 60 Hz, 1 min	2500	V	

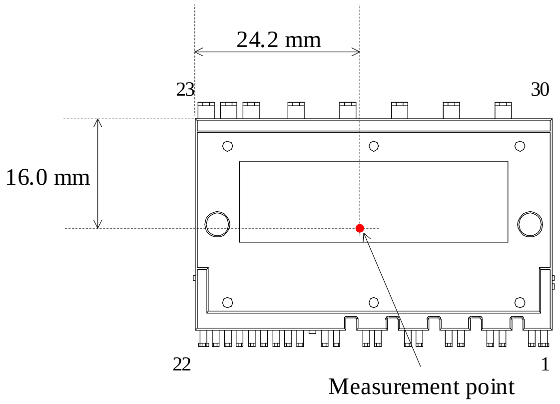

Figure 2-1. SAM265M30AA1 Case Temperature Measurement Point

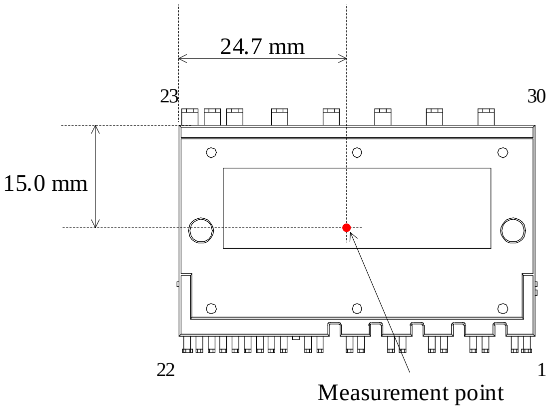

Figure 2-2. SAM265M50AA1 Case Temperature Measurement Point

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[2] Refers to the junction temperature of each chip built in the IC, including the control MICs, IGBTs, and freewheeling diodes.

[3] Refers to a case temperature measured during IC operation.

[4] Refers to voltage conditions to be applied between all of the pins and the case. All the pins have to be shorted.

3. Recommended Operating Conditions

Unless specifically noted, T_C = −40 °C to 125 °C, $V_{P(DC)}$ = 300 V, V_{VCCHx} = V_{VCCL} = $V_{VBx\text{-}VSx}$ = 15 V, R_{FO} = 10 kΩ, C_{FO} = 0 μF, V_{FO_PU} = 5 V.

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Remarks
Main Supply Voltage (DC)	$V_{P(DC)}$	P–Nx		150	300	450	V	
Phase Current (Effective Value) (1)	$I_{C(RMS)}$	(2)	f_{PWM} = 5 kHz	—	—	21	A	SAM265M30AA1
			f_{PWM} = 10 kHz	—	—	17		
			f_{PWM} = 15 kHz	—	—	14		
			f_{PWM} = 20 kHz	—	—	12		
		(2)	f_{PWM} = 5 kHz	—	—	33	A	SAM265M50AA1
			f_{PWM} = 10 kHz	—	—	25		
			f_{PWM} = 15 kHz	—	—	20		
			f_{PWM} = 20 kHz	—	—	17		
VCCHx Pin Voltage	V_{VCCHx}	VCCHx–GND		13.5	15.0	16.5	V	
VCCL Pin Voltage	V_{VCCL}	VCCL–GND		13.5	15.0	16.5	V	
VBx–VSx Pin Voltage	$V_{VBx\text{-}VSx}$	VBx–VSx		13.0	15.0	18.5	V	
Dead Time of Input Signal	t_{DEAD}	INHx, INLx		1.5	—	—	μs	
PWM Control Frequency	f_{PWM}			5	10	20	kHz	
INxH Pin Input Pulse Width (On)	$t_{INHX(ON)}$			1.5	—	—	μs	
INxH Pin Input Pulse Width (Off)	$t_{INHX(OFF)}$			1.5	—	—	μs	
INxL Pin Input Pulse Width (On)	$t_{INLX(ON)}$			1.5	—	—	μs	
INxL Pin Input Pulse Width (Off)	$t_{INLX(OFF)}$			1.5	—	—	μs	
P Pin Capacitor 1	$C_{P(DC)}$			22	47	—	μF	
P Pin Capacitor 2	C_S	Ceramic capacitor		0.1	—	—	μF	
VCCHx/VCCL Pin Capacitor 1	C_{VCC1}			22	47	—	μF	
VCCHx/VCCL Pin Capacitor 2	C_{VCC2}	Ceramic capacitor		0.47	1.0	2.2	μF	
Bootstrap Capacitor 1	C_{BS1}			4.7	10	100	μF	SAM265M30AA1
				4.7	22	100	μF	SAM265M50AA1
Bootstrap Capacitor 2	C_{BS2}	Ceramic capacitor		0.47	1.0	2.2	μF	

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(1) The maximum value of the phase current varies depending on application conditions.

(2) Sine wave, modulation index = 1, power factor = 0.8, −40 °C ≤ T_C ≤ 100 °C, −40°C ≤ T_J ≤ 150 °C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
External VCC Supply Output Current	I_{VCC}	f_{PWM} = 5 kHz	18	—	—	mA	SAM265M30AA1
		f_{PWM} = 10 kHz	24	—	—		
		f_{PWM} = 15 kHz	30	—	—		
		f_{PWM} = 20 kHz	36	—	—		
		f_{PWM} = 5 kHz	24	—	—	mA	SAM265M50AA1
		f_{PWM} = 10 kHz	36	—	—		
		f_{PWM} = 15 kHz	48	—	—		
		f_{PWM} = 20 kHz	60	—	—		
VCCxH/VCCL Pin Zener Diode Breakdown Voltage	$V_{Z\text{-}DVCC}$	I_Z = 1 mA	16.5	18.2	20.0	V	
FO Pin Pull-up Resistor	R_{FO}		5.5	10.0	33.0	kΩ	
FO Pin Pull-up Voltage	V_{FO_PU}		3.0	5.0	5.5	V	
FO Pin Capacitor	C_{FO}		—	1000	3300	pF	
CFO Pin Capacitor	C_{CFO}		0.01	0.10	1.00	µF	
Shunt Resistor[3]	R_S	OCP operating current: 30 A to 60 A	9.0	12.2	15.3	mΩ	SAM265M30AA1
		OCP operating current: 50 A to 100 A	5.4	7.3	9.2	mΩ	SAM265M50AA1
OCP RC Filter Time Constant	t_{RFCF}	$t_{RFCF} = R_F \times C_F$	0.3	—	1.5	µs	
Thermistor Operating Current	I_{TH}		—	—	0.2	mA	

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[3] Should be a low-inductance resistor.

4. Electrical Characteristics

Unless specifically noted, T_C = −40 °C to 125 °C, $V_{P(DC)}$ = 300 V, V_{VCCHx} = V_{VCCL} = $V_{VBx\text{-}VSx}$ = 15 V, R_{FO} = 10 kΩ, C_{FO} = 0 μF, V_{FO_PU} = 5 V. The shipping test is performed at T_A = 25 °C and 125 °C for the electrical characteristics shown below (except for the parameters guaranteed by design).

4.1. Characteristics of Control Parts

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Power Supply Operation							
VCCL Pin Operating Voltage	V_{VCCL_H}		11.2	12.6	13.3	V	UVLO recovery voltage
VCCL Pin Operation Stop Voltage	V_{VCCL_L}		10.7	12.1	12.8	V	UVLO detection voltage
VCCL Pin Hysteresis	V_{VCCL_HYS}		—	0.5	—	V	
VBx−VSx Operating Voltage	$V_{VBx\text{-}VSx\_H}$		11.0	12.1	12.8	V	UVLO recovery voltage
VBx−VSx Operation Stop Voltage	$V_{VBx\text{-}VSx\_L}$		10.5	11.6	12.3	V	UVLO detection voltage
VBx−VSx Hysteresis	$V_{VBx\text{-}VSx\_HYS}$		—	0.5	—	V	
VCCHx Pin Input Current	I_{VCCHX}	V_{INHx} = 0 V, each pin	—	1.4	2.0	mA	
		V_{INHx} = 5 V, each pin	—	1.4	2.0		
VCCL Pin Input Current	I_{VCCL}	V_{INLx} = 0 V	—	1.9	3.2	mA	
		V_{INLx} = 5 V	—	1.9	3.2		
VBx−VSx Pin Input Current	$I_{VBx\text{-}VSx}$	$V_{VBx\text{-}VSx}$ = 15 V, V_{INHx} = 0 V; 1-phase operation	—	0.09	0.30	mA	
		$V_{VBx\text{-}VSx}$ = 15 V, V_{INHx} = 5 V; 1-phase operation	—	0.12	0.30		
Input Signal							
INHx Pin High-level Input Threshold Voltage	V_{INHx_H}		—	2.0	2.5	V	
INHx Pin Low-level Input Threshold Voltage	V_{INHx_L}		1.0	1.5	—	V	
INHx Pin Hysteresis	V_{INHx_HYS}		—	0.5	—	V	
INLx Pin High-level Input Threshold Voltage	V_{INLx_H}		—	2.0	2.5	V	
INLx Pin Low-level Input Threshold Voltage	V_{INLx_L}		1.0	1.5	—	V	
INLx Pin Hysteresis	V_{INLx_HYS}		—	0.5	—	V	
INHx Pin Input Current	I_{INHx}	V_{INHx} = 5 V, each pin	—	0.25	0.50	mA	
INLx Pin Input Current	I_{INLx}	V_{INLx} = 5 V, each pin	—	0.25	0.50	mA	
Fault Signal Output, Shutdown Signal Input							
FO Pin Shutdown Release Voltage	V_{FO_H}		—	2.0	2.5	V	
FO Pin Shutdown Threshold Voltage	V_{FO_L}		1.0	1.5	—	V	
FO Pin Shutdown Hysteresis	V_{FO_HYS}		—	0.5	—	V	
FO Pin Output Voltage in Normal Operation	V_{FO_H}	V_{FO_PU} = 5 V, R_{FO} = 10 kΩ, V_{OCP} = 0 V	4.8	5.0	—	V	
FO Pin Fault Signal Output Voltage	V_{FO_L}	V_{FO_PU} = 5 V, R_{FO} = 10 kΩ, V_{OCP} = 1 V	—	0.09	0.50	V	

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
FO Pin OCP Hold Time[1]	t_{FO}	C_{CFO} = 0 µF	0.012	0.030	0.060	ms	
		C_{CFO} = 0.001 µF	0.20	0.32	0.44	ms	
		C_{CFO} = 0.01 µF	2.0	3.2	4.4	ms	
		C_{CFO} = 0.1 µF	20	32	44	ms	
		C_{CFO} = 1 µF	200	320	440	ms	
Protection							
OCP Pin Overcurrent Detection Voltage	V_{OCP_H}		0.46	0.50	0.54	V	
OCP Pin Overcurrent Release Voltage	V_{OCP_L}		0.32	0.38	0.44	V	
OCP Pin Overcurrent Hysteresis	V_{OCP_HYS}		—	0.12	—	V	
OCP Pin Detection Delay Time[2]	t_{OCP_DELAY}	[3]	—	0.7	1.5	µs	
OCP Pin Input Current	I_{OCP}	V_{OCP} = 0.5 V	—	0	—	mA	

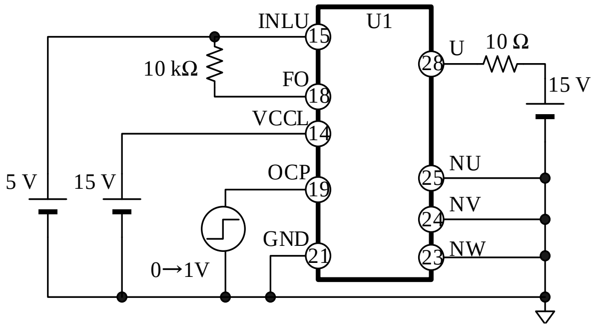

Figure 4-1. Measurement Circuit for OCP Pin Detection Delay Time

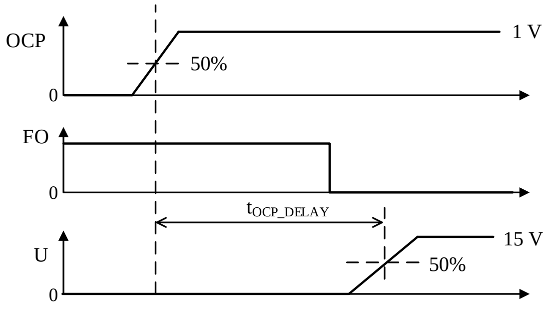

Figure 4-2. OCP Pin Detection Delay Time Definition

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[1] The shipping test is performed with the condition at C_{CFO} = 0.01 µF only.

[2] Guaranteed by design.

[3] For the measurement circuit for the OCP Pin Detection Delay Time, see Figure 4-1 (all the pins that are not represented in the figure are open). Figure 4-2 provides the definition of the OCP Pin Detection Delay Time.

4.2. Bootstrap Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Bootstrap Diode Forward Voltage Drop	V_{F_BS}	I_{F_BS} = 0.1 A	2.0	3.0	4.0	V	Voltage drop in series resistors included; see Figure 4-3
Bootstrap Diode Series Resistor*	R_{S_BS}		12	20	28	Ω	

* Guaranteed by design.

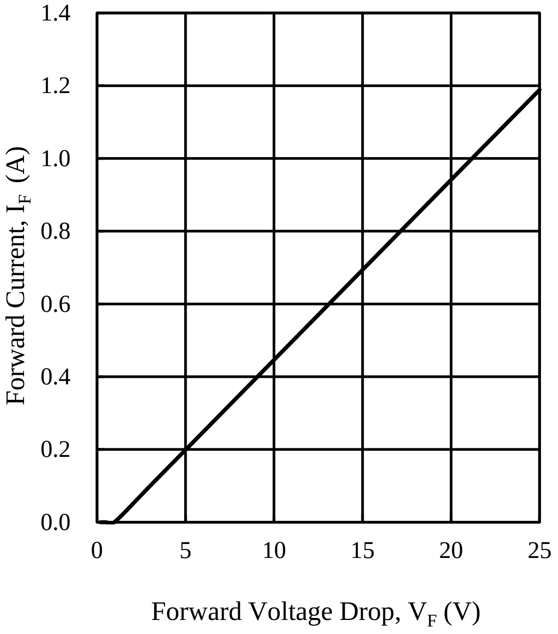

Figure 4-3. Bootstrap Diode: I_F vs. V_F (T_J = 25 °C)

4.3. Thermistor Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Thermistor Resistance(1)(2)	R_{25}	T_{TH} = 25 °C	—	100.0	—	kΩ	
Thermistor B Constant(1)	$B_{25\text{-}85}$	T_{TH} = 25 °C, 85 °C	—	4395	—	K	

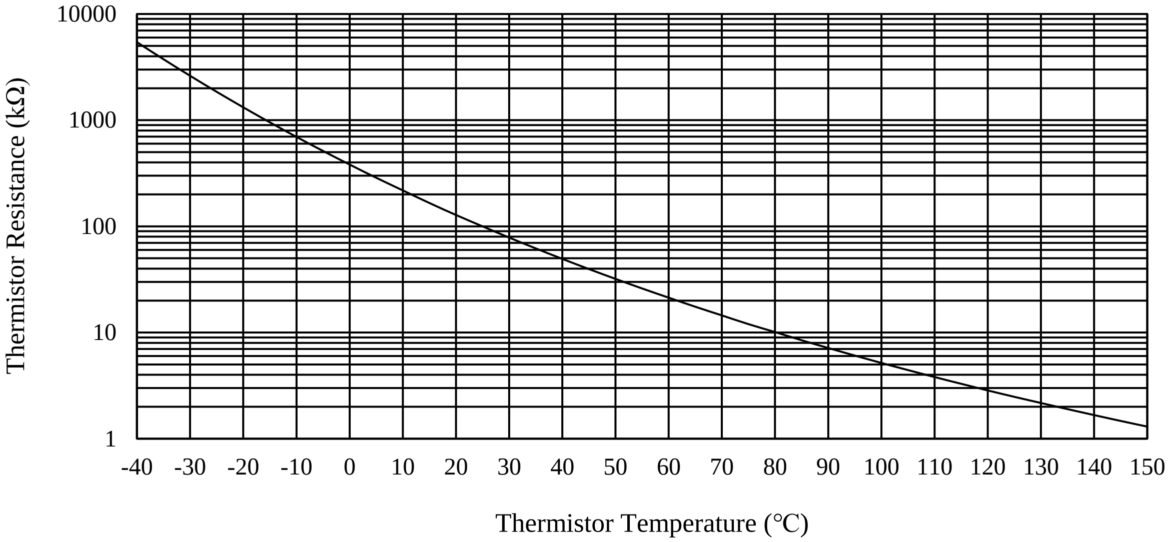

Figure 4-4. Reference Thermistor Resistance

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(1) Guaranteed by design.

(2) For the reference thermistor resistance, see Figure 4-4 and Table 4-1.

Table 4-1. Reference Thermistor Resistance

Thermistor Temperature (°C)	Thermistor Resistance Typ. (kΩ)
−40	5427
−35	3748
−30	2619
−25	1850
−20	1321
−15	954
−10	696
−5	513
0	382
5	287
10	218
15	166
20	128
25	100
30	78.4
35	62.0
40	49.4
45	39.6
50	32.0
55	26.0
60	21.3
65	17.5
70	14.5
75	12.0
80	10.1
85	8.46
90	7.15
95	6.07
100	5.17
105	4.43
110	3.81
115	3.29
120	2.85
125	2.48
130	2.17
135	1.90
140	1.67
145	1.47
150	1.30

4.4. Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Junction-to-Case Thermal Resistance[3][4]	$R_{(J\text{-}C)Q}$[5]	1 element operating (IGBT)	—	—	1.45	°C/W	SAM265M30AA1
			—	—	1.0		SAM265M50AA1
	$R_{(J\text{-}C)F}$[6]	1 element operating (freewheeling diode)	—	—	3.0	°C/W	SAM265M30AA1
			—	—	2.3		SAM265M50AA1

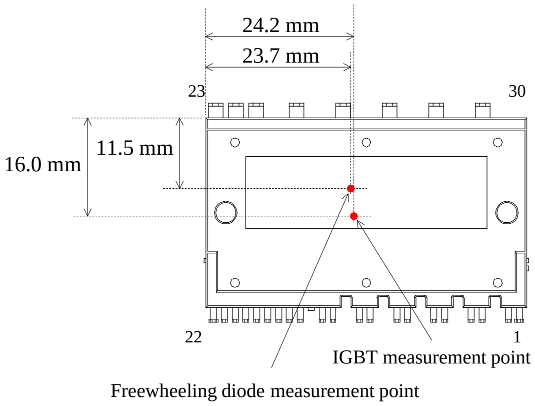

Figure 4-5. Case Temperature Measurement Point: SAM265M30AA1

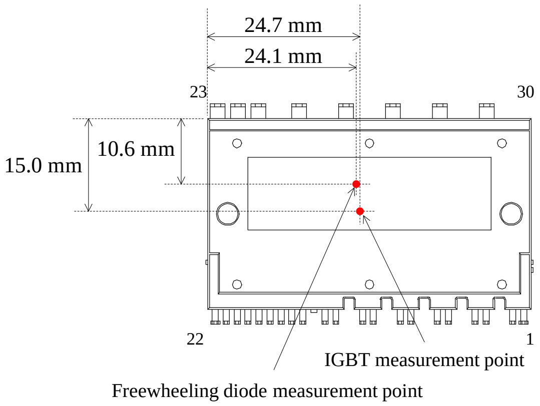

Figure 4-6. Case Temperature Measurement Point: SAM265M50AA1

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[3] Guaranteed by design.

[4] Refers to a case temperature at the measurement point described in Figure 4-5 or Figure 4-6.

[5] Refers to steady-state thermal resistance between the junction of the built-in IGBTs and the case.

[6] Refers to steady-state thermal resistance between the junction of the built-in freewheeling diodes and the case.

4.5. Transistor Characteristics

Figure 4-7 provides the definitions of switching characteristics described in this and the following sections.

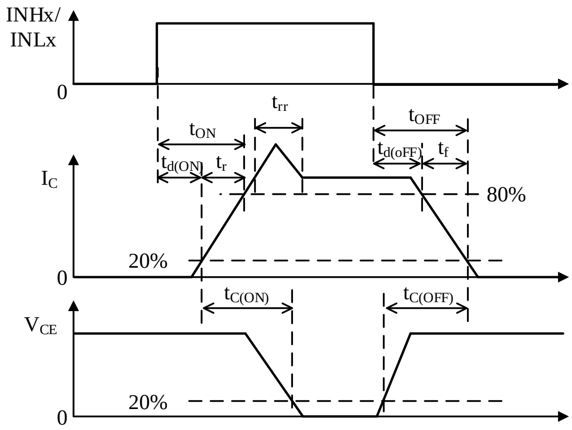

Figure 4-7. Switching Characteristics Definitions

4.5.1. SAM265M30AA1

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 650 V, T_J = 25 °C	—	—	0.1	mA
		V_{CE} = 650 V, T_J = 125 °C	—	—	0.5	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 30 A, T_J = 25 °C	—	1.7	2.2	V
		I_C = 30 A, T_J = 125 °C	—	1.8	2.3	V
Diode Forward Voltage Drop	V_F	I_F = 30 A, T_J = 25 °C	—	1.9	2.4	V
High-side Switching						
Diode Reverse Recovery Time*	t_{rr}	$V_{P(DC)}$ = 300 V, I_C = 30 A, V_{IN} = 0 ↔ 5 V, T_J = 25 °C; inductive load	—	0.14	—	μs
Turn-on Time*	t_{ON}		—	0.99	—	μs
Turn-on Delay Time*	$t_{d(ON)}$		—	0.90	—	μs
Turn-on Rise Time*	t_r		—	0.09	—	μs
Turn-on Switching Time*	$t_{C(ON)}$		—	0.17	—	μs
Turn-off Time*	t_{OFF}		—	1.16	—	μs
Turn-off Delay Time*	$t_{d(OFF)}$		—	1.02	—	μs
Turn-off Fall Time*	t_f		—	0.14	—	μs
Turn-off Switching Time *	$t_{C(OFF)}$		—	0.24	—	μs
Low-side Switching						
Diode Reverse Recovery Time *	t_{rr}	$V_{P(DC)}$ = 300 V, I_C = 30 A, V_{IN} = 0 ↔ 5 V, T_J = 25 °C; inductive load	—	0.12	—	μs
Turn-on Time*	t_{ON}		—	0.66	—	μs
Turn-on Delay Time*	$t_{d(ON)}$		—	0.57	—	μs
Turn-on Rise Time*	t_r		—	0.09	—	μs
Turn-on Switching Time*	$t_{C(ON)}$		—	0.16	—	μs
Turn-off Time*	t_{OFF}		—	0.86	—	μs
Turn-off Delay Time*	$t_{d(OFF)}$		—	0.72	—	μs
Turn-off Fall Time*	t_f		—	0.14	—	μs
Turn-off Switching Time *	$t_{C(OFF)}$		—	0.22	—	μs

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* Guaranteed by design.

4.5.2. SAM265M50AA1

Parameter	Symbol	Conditions	Min.	Typ.	Max.	単位
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 650 V, T_J = 25 °C	—	—	0.15	mA
		V_{CE} = 650 V, T_J = 125 °C	—	—	0.75	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 50 A, T_J = 25 °C	—	1.7	2.2	V
		I_C = 50 A, T_J = 125 °C	—	1.8	2.3	V
Diode Forward Voltage Drop	V_F	I_F = 50 A, T_J = 25 °C	—	1.9	2.4	V
High-side Switching						
Diode Reverse Recovery Time*	t_{rr}	$V_{P(DC)}$ = 300 V, I_C = 50 A, V_{IN} = 0 ↔ 5 V, T_J = 25 °C; inductive load	—	0.20	—	μs
Turn-on Time*	t_{ON}		—	0.80	—	μs
Turn-on Delay Time*	$t_{d(ON)}$		—	0.70	—	μs
Turn-on Rise Time*	t_r		—	0.10	—	μs
Turn-on Switching Time*	$t_{C(ON)}$		—	0.15	—	μs
Turn-off Time*	t_{OFF}		—	1.10	—	μs
Turn-off Delay Time*	$t_{d(OFF)}$		—	0.90	—	μs
Turn-off Fall Time*	t_f		—	0.20	—	μs
Turn-off Switching Time *	$t_{C(OFF)}$		—	0.25	—	μs
Low-side Switching						
Diode Reverse Recovery Time *	t_{rr}	$V_{P(DC)}$ = 300 V, I_C = 50 A, V_{IN} = 0 ↔ 5 V, T_J = 25 °C; inductive load	—	0.25	—	μs
Turn-on Time*	t_{ON}		—	0.60	—	μs
Turn-on Delay Time*	$t_{d(ON)}$		—	0.50	—	μs
Turn-on Rise Time*	t_r		—	0.10	—	μs
Turn-on Switching Time*	$t_{C(ON)}$		—	0.20	—	μs
Turn-off Time*	t_{OFF}		—	0.80	—	μs
Turn-off Delay Time*	$t_{d(OFF)}$		—	0.60	—	μs
Turn-off Fall Time*	t_f		—	0.20	—	μs
Turn-off Switching Time *	$t_{C(OFF)}$		—	0.25	—	μs

---

* Guaranteed by design.

5. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Heatsink Mounting Screw Torque[1]	[2]	0.64	0.80	0.96	N·m
		6.6	8.2	9.8	kgf·cm
Flatness of Heatsink Attachment Area[1]	See Figure 5-1.	0	—	100	μm
Package Weight[1]		—	23	—	g

[1] Guaranteed by design.

[2] Requires using a metric screw of M3 and a plain washer of 7 mm (φ). For more details about screw tightening, see Section 14.2.

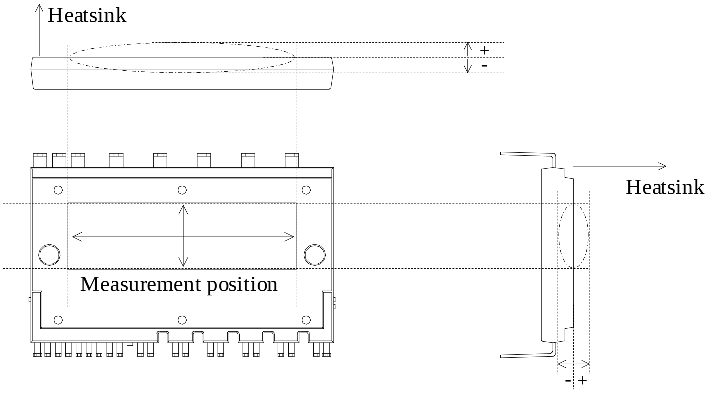


Figure 5-1. Flatness Measurement Position

6. Insulation Distance

Parameter	Conditions	Min.	Typ.	Max.	Unit
Clearance[1]	Between heatsink and leads. See Figure 6-1.	3.0	3.1	—	mm
Creepage[1][2]		4.2	4.6	—	mm

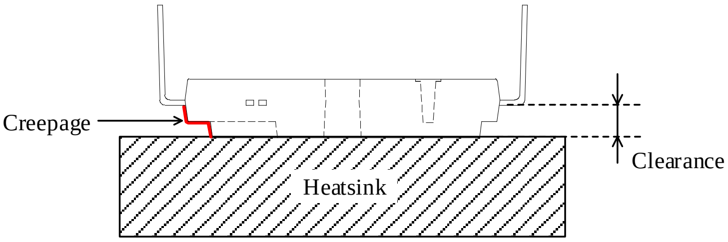


Figure 6-1. Insulation Distance Definitions

[1] Guaranteed by design.

[2] Refers to when a heatsink to be mounted is flat. If your application requires a clearance exceeding the maximum distance given above, use an alternative (e.g., a convex heatsink) that will meet the target requirement.

7. Truth Table

Table 7-1 is a truth table that provides the logic level definitions of operation modes.

In the case where INHx and INLx signals in each phase are high at the same time, both the high- and low-side IGBTs become on (simultaneous on-state).

Table 7-1. Truth Table for Operation Modes

Mode	INHx	INLx	High-side IGBT	Low-side IGBT	FO Pin Output
Normal Operation	L	L	OFF	OFF	H
	H	L	ON	OFF	
	L	H	OFF	ON	
	H	H	ON	ON	
External Shutdown Signal Input FO = L	L	L	OFF	OFF	—
	H	L	ON	OFF	
	L	H	OFF	OFF	
	H	H	ON	OFF	
VBx Pin Undervoltage Lockout Operation (UVLO_VBx)	L	L	OFF	OFF	H
	H	L	OFF	OFF	
	L	H	OFF	ON	
	H	H	OFF	ON	
VCCL Pin Undervoltage Lockout Operation (UVLO_VCCL)	L	L	OFF	OFF	L
	H	L	ON	OFF	
	L	H	OFF	OFF	
	H	H	ON	OFF	
Overcurrent Protection (OCP)	L	L	OFF	OFF	L
	H	L	ON	OFF	
	L	H	OFF	OFF	
	H	H	ON	OFF	

8. Block Diagram

Figure 8-1 shows a block diagram, Figure 8-2 to Figure 8-4 show the internal circuit diagrams of the INHx or INLx pin, the FO pin, and the OCP pin.

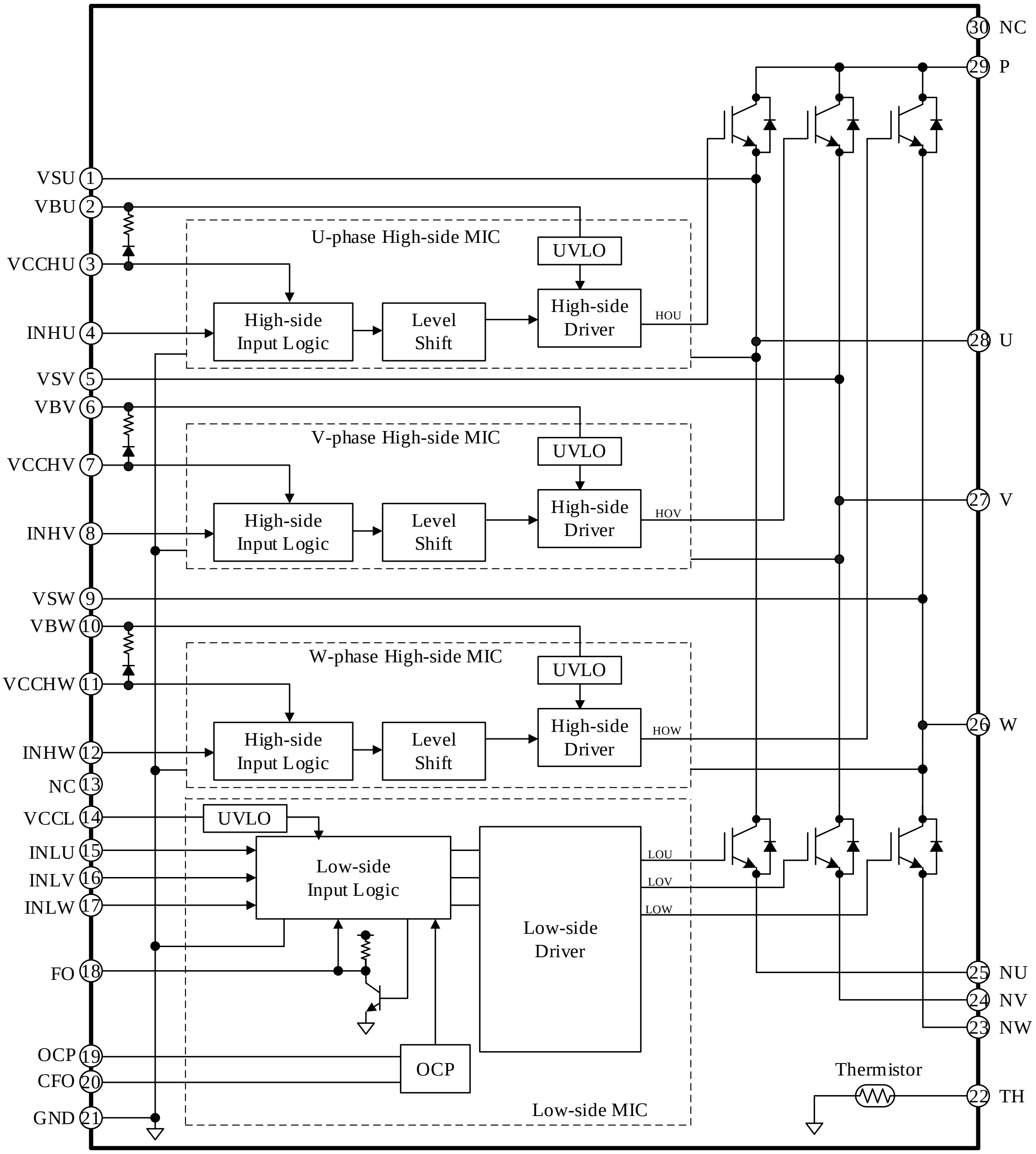


Figure 8-1. Block Diagram

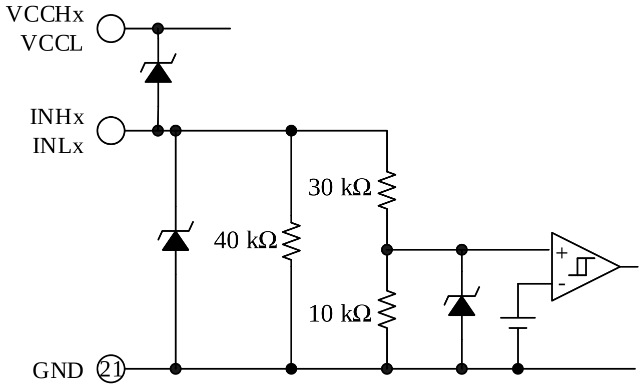


Figure 8-2. Internal Circuit Diagram of INHx or INLx Pin

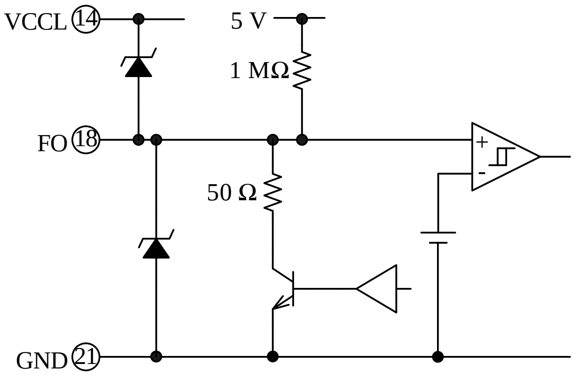


Figure 8-3. Internal Circuit Diagram of FO Pin

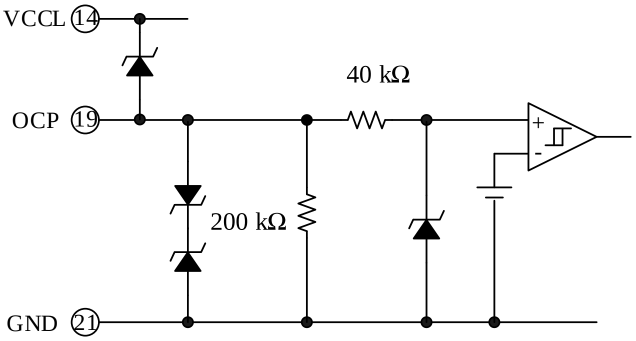
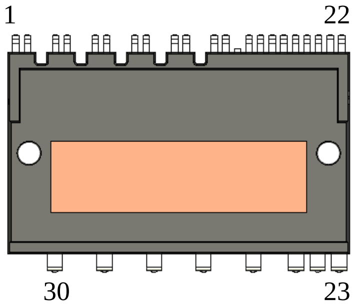


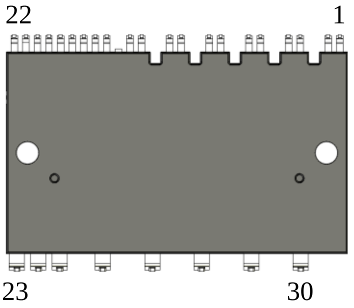
Figure 8-4. Internal Circuit Diagram of OCP Pin

9. Pin Configuration Definitions

Top View (Heatsink Side)



Bottom View (Branding Side)



Pin Number	Pin Name	Description
1	VSU	U-phase high-side floating supply ground
2	VBU	U-phase high-side floating supply voltage input
3	VCCHU	U-phase high-side logic supply voltage input
4	INHU	Logic input for U-phase high-side gate driver
5	VSV	V-phase high-side floating supply ground
6	VBV	V-phase high-side floating supply voltage input
7	VCCHV	V-phase high-side logic supply voltage input
8	INHV	Logic input for V-phase high-side gate driver
9	VSW	W-phase high-side floating supply ground
10	VBW	W-phase high-side floating supply voltage input
11	VCCHW	W-phase high-side logic supply voltage input
12	INHW	Logic input for W-phase high-side gate driver
13*	NC	(No connection)
14	VCCL	Low-side logic supply voltage input
15	INLU	Logic input for U-phase low-side gate driver
16	INLV	Logic input for V-phase low-side gate driver
17	INLW	Logic input for W-phase low-side gate driver
18	FO	Fault signal output and shutdown signal input
19	OCP	Input for overcurrent protection
20	CFO	Capacitor connection for OCP hold time setting
21	GND	Logic ground
22	TH	Thermistor output
23	NW	W-phase low-side IGBT emitter
24	NV	V-phase low-side IGBT emitter
25	NU	U-phase low-side IGBT emitter
26	W	W-phase output
27	V	V-phase output
28	U	U-phase output
29	P	Positive DC bus supply voltage
30	NC	(No connection)

---

* Pin trimmed.

10. Typical Application

CR filters and Zener diodes should be added to your application as needed. This is to protect each pin against surge voltages causing malfunctions, and to avoid the IC being used under the conditions exceeding the absolute maximum ratings where critical damage is inevitable. Then, check all the pins thoroughly under actual operating conditions to ensure that your application works flawlessly.

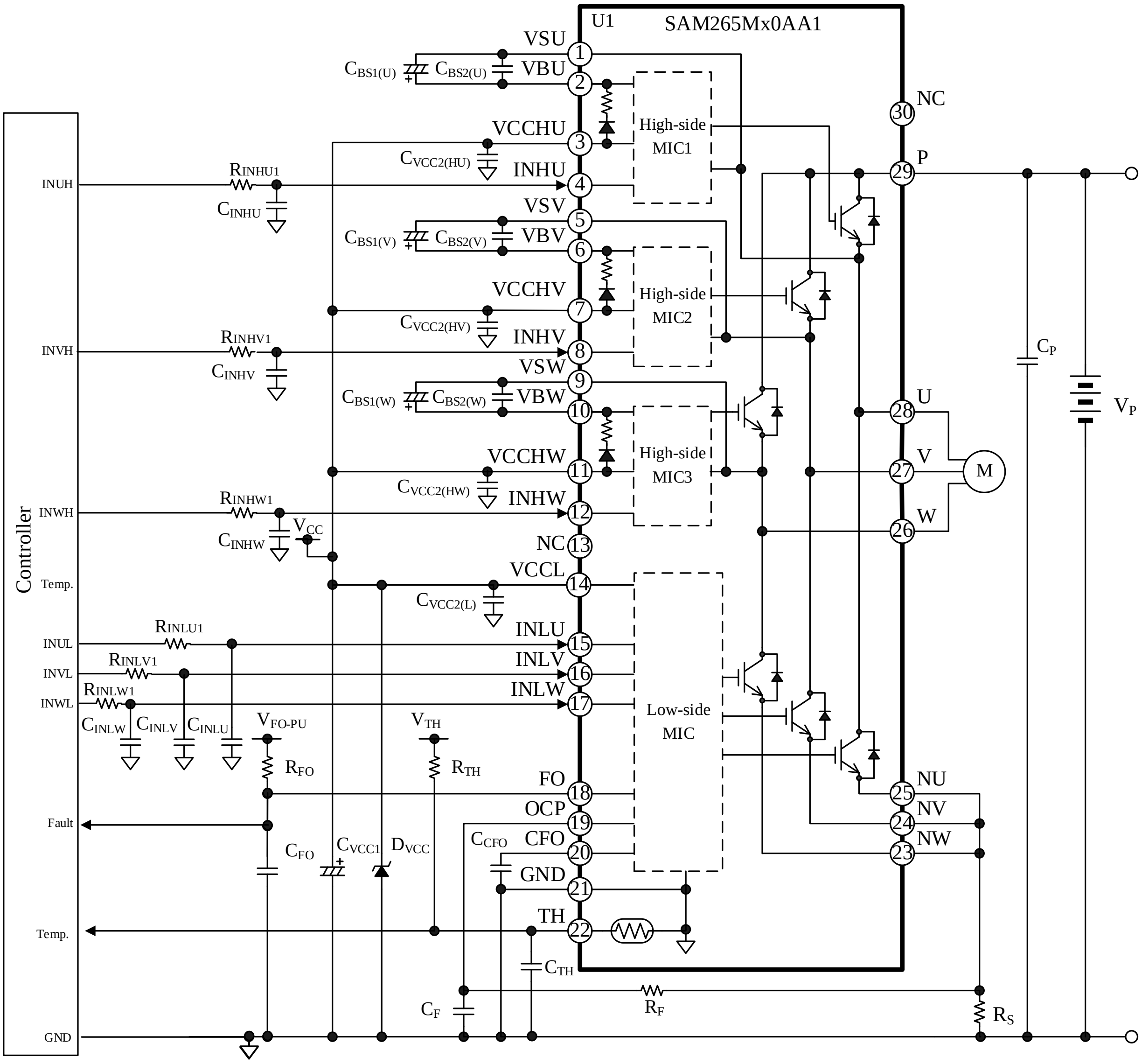


Figure 10-1. Typical Application Using a Single Shunt Resistor

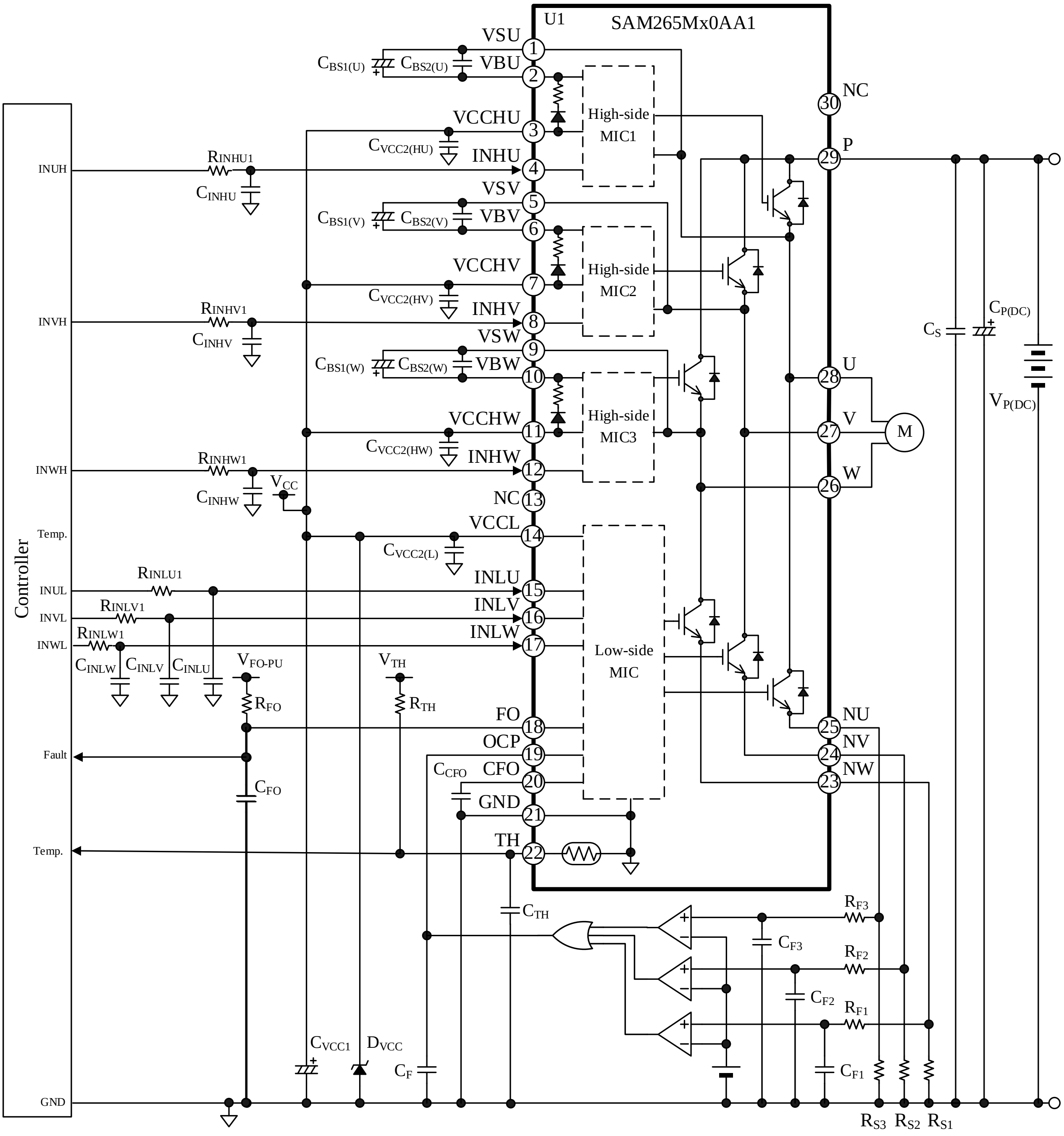
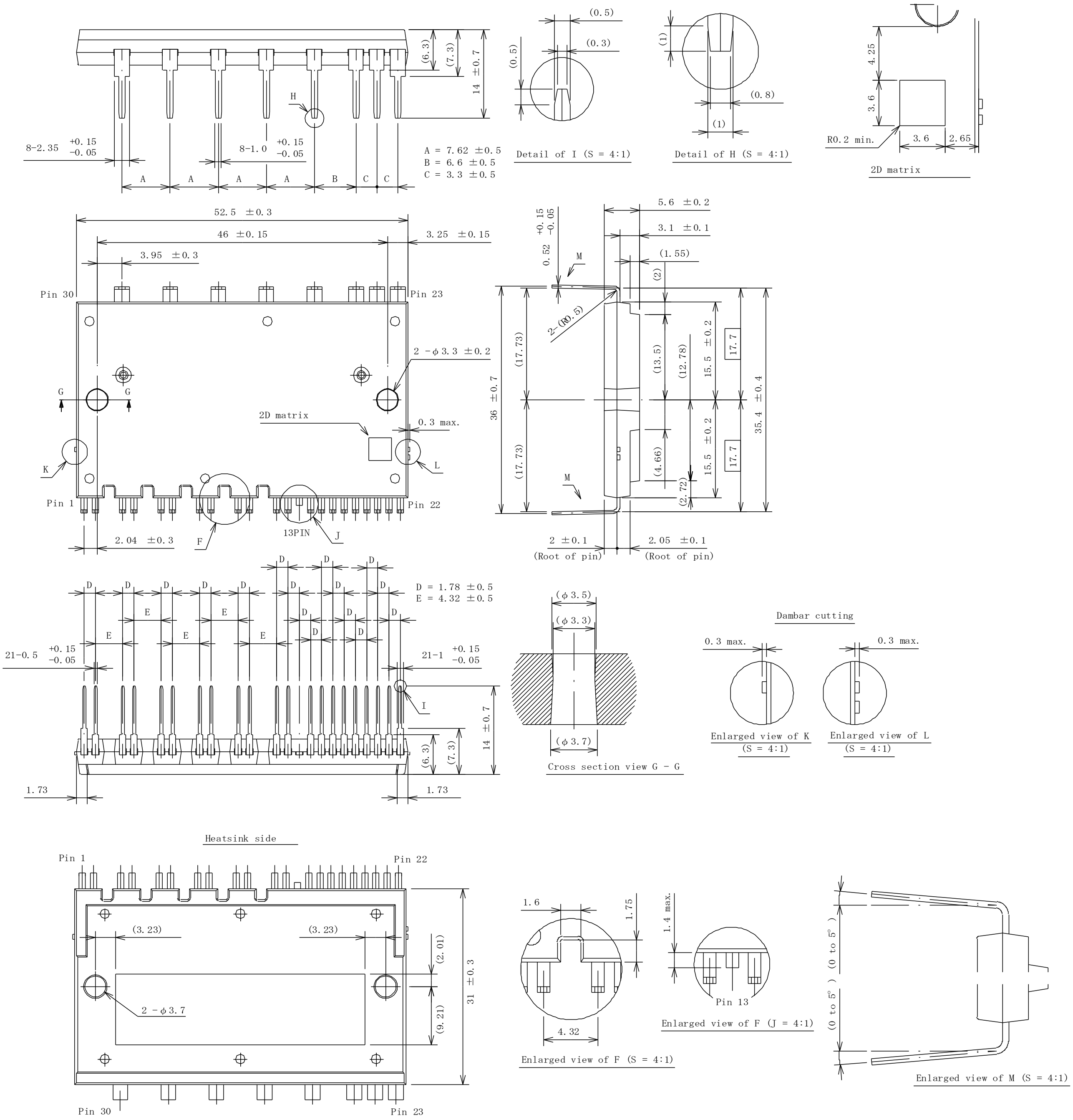


Figure 10-2. Typical Application Using Three Shunt Resistors

11. Physical Dimensions

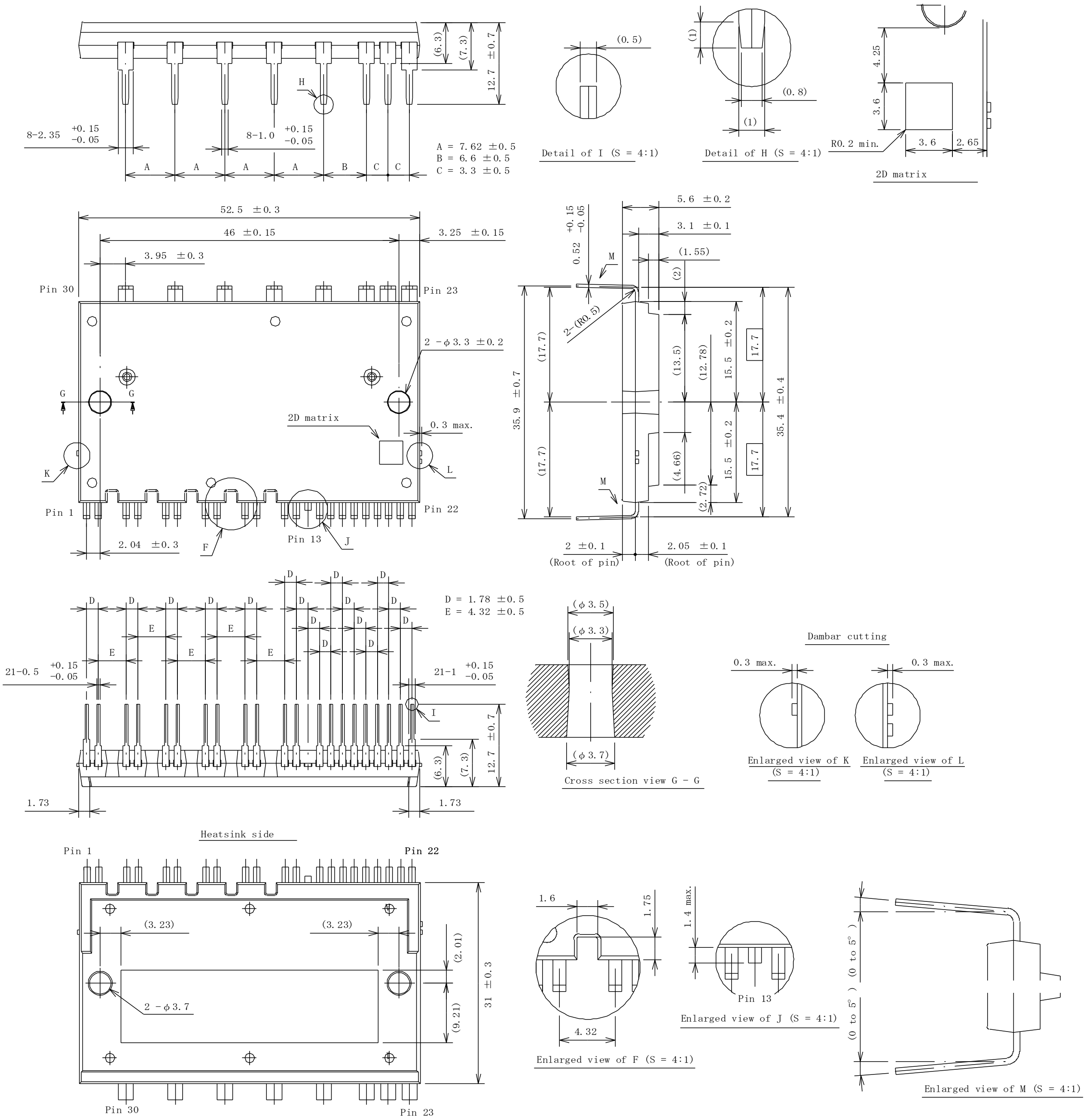
11.1. DIP30 (Leadform: 2540)



NOTES:

- Dimensions in millimeters
- Pb-free (RoHS compliant)

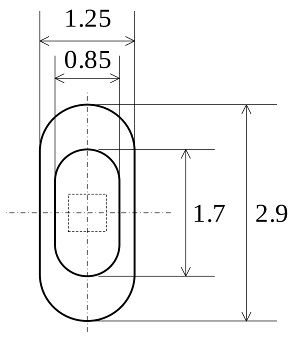
11.2. DIP30 (Leadform: 2541)



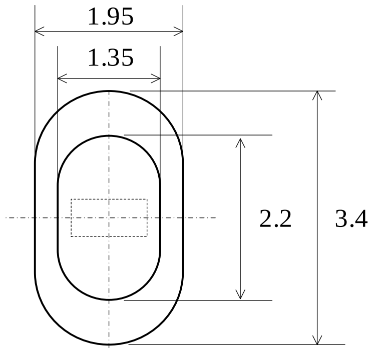
NOTES:

- Dimensions in millimeters
- Pb-free (RoHS compliant)

11.3. Reference PCB Hole Sizes

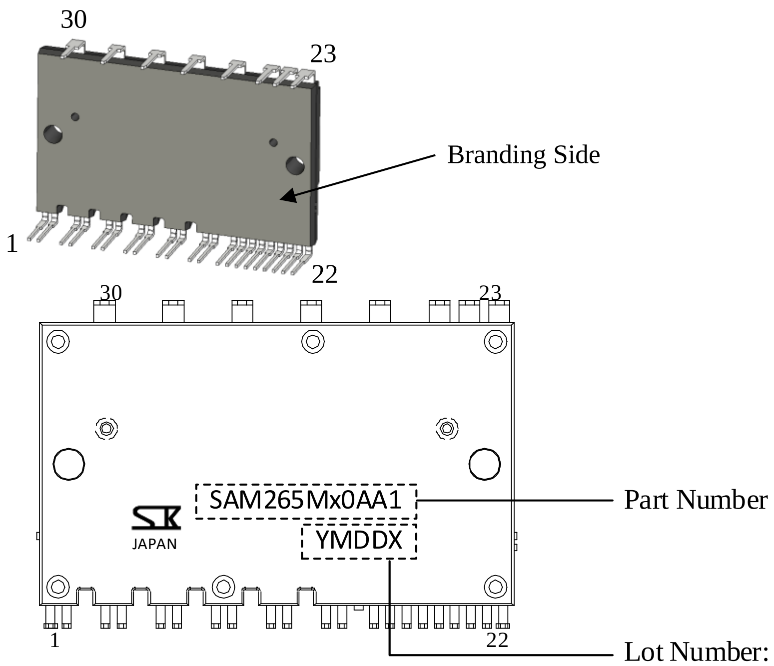


Pins 1 to 22



Pins 23 to 30

12. Marking Diagram



Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
DD is the day of the month (01 to 31)
X is the control number

13. Functional Descriptions

Unless specifically noted, this section uses the following definitions:

- All the characteristic values given in this section are typical values.
- In the following functional descriptions, "HOx" denotes a gate input signal on the high-side IGBT, whereas "LOx" denotes a gate input signal on the low-side IGBT.
- For pin and peripheral component descriptions, this section employs a notation system that denotes a pin name with the arbitrary letter "x", depending on context. Thus, "R_{Sx}" is used when referring to any or all of the resistors R_{S1}, R_{S2}, and R_{S3}.

13.1. Turning On and Off the IC

The procedures listed below provide recommended startup and shutdown sequences. To turn on the IC properly, do not apply any voltage on the INHx and INLx pins until the VCCL pin voltage has reached a stable state ($V_{VCCL\_H} \geq 13.3$ V).

It is required to fully charge bootstrap capacitors, $C_{BS1(x)}$ and $C_{BS2(x)}$, at startup (see Section 13.2.4).

To turn off the IC, set the INHx and INLx pins to logic low (or "L"), and then decrease the VCCL pin voltage.

13.2. Pin Descriptions

13.2.1. P

This is the input pin for the main supply voltage, i.e., the positive DC bus. All of the IGBT collectors of the high-side are connected to this pin. Voltages between the P and Nx pins should be set within the recommended range of the main supply voltage, $V_{P(DC)}$, given in Section 3.

To suppress surge voltages, put a bypass capacitor of ≥0.1 μF, C_S, near the P pin and an electrolytic capacitor, $C_{P(DC)}$, with a minimal length of PCB traces to the P pin.

13.2.2. U, V, and W

These pins are the outputs of the three phases, and serve as the connection terminals to the 3-phase motor. The U, V, and W pins are internally connected to the VSU, VSV, and VSW pins, respectively.

13.2.3. NU, NV, and NW

These are the emitter pins of the low-side IGBTs and are externally connected to shunt resistors, R_{Sx}.

When connecting a shunt resistor, place it as near as possible to the IC with a minimum length of traces to the Nx and GND pins.

13.2.4. VBU, VBV, and VBW

These are the inputs of the high-side floating power supplies for the individual phases.

Voltages across the VBx and VSx pins should be maintained within the defined range (i.e., the VBx–VSx Pin Voltage, $V_{VBx\text{-}VSx}$) in Section 3.

In each phase, a bootstrap capacitor, $C_{BS1(x)}$, should be connected between the VBx and VSx pins. For proper startup, turn on the low-side transistor first, then fully charge the bootstrap capacitor, $C_{BS1(x)}$. For the capacitance of the bootstrap capacitors, $C_{BS1(x)}$, choose the values that satisfy Equations (1) and (2). Note that capacitance tolerance and DC bias characteristics must be taken into account when you choose appropriate values for $C_{BS1(x)}$.

SAM265M30AA1:

$$C_{BS1(x)}\ (\mu F) > (60 \times f_{PWM}\ (kHz) + 90) \times t_{L(OFF)}\ (s) \tag{1}$$

SAM265M50AA1:

$$C_{BS1(x)}\ (\mu F) > (110 \times f_{PWM}\ (kHz) + 90) \times t_{L(OFF)}\ (s)$$

$$4.7\ \mu F \leq C_{BS1(x)} \leq 100\ \mu F \tag{2}$$

In Equation (1), let $t_{L(OFF)}$ be the maximum off-time of the low-side transistor (i.e., the non-charging time of $C_{BS1(x)}$), measured in seconds.

Even while the high-side transistor is not on, voltage across the bootstrap capacitor keeps decreasing due to power dissipation in the IC. When the VBx pin voltage decreases to $V_{VBx\text{-}VSx\_L}$ or less, the VBx pin undervoltage lockout (UVLO_VBx) starts operating (see Section 13.3.3.1). Therefore, actual board checking should be done thoroughly to validate that voltage across the VBx pin maintains over 12.3 V ($V_{VBx} > V_{VBx\text{-}VSx\_L}$) during a low-frequency operation such as a startup period.

As Figure 13-1 shows, bootstrap diodes, $D_{B(x)}$, and current-limiting resistors, $R_{B(x)}$, are internally placed in series between the VCCHx and VBx pins. Time constant for the charging time of $C_{BS1(x)}$, τ, can be computed by Equation (3):

$$\tau = C_{BS1(x)} \times R_{B(x)}\ , \tag{3}$$

where $C_{BS1(x)}$ is the optimized capacitance of the bootstrap capacitor, and $R_{B(x)}$ is the resistance of the current-limiting resistor (20 Ω ± 20%).

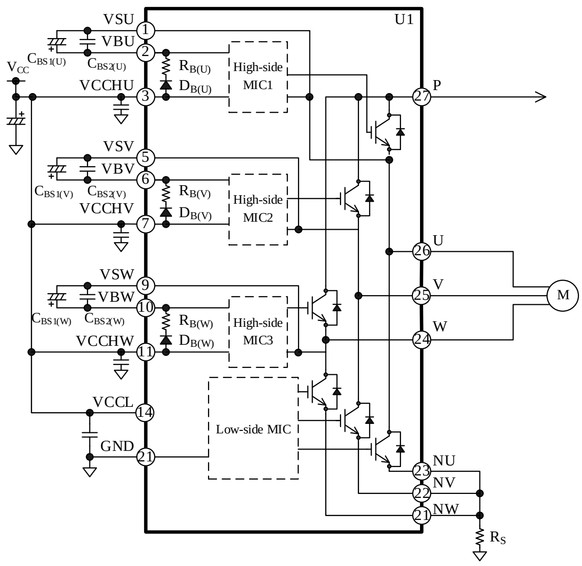


Figure 13-1. Bootstrap Circuit

Figure 13-2 shows an internal level-shifting circuit. And Figure 13-3 shows operational waveforms of the level-shifting circuit. A high-side output signal, HOx, is generated according to an input signal on the INHx pin. When an input signal on the INHx pin transits from low to high (rising edge), a “Set” signal is generated. When the INHx input signal transits from high to low (falling edge), a “Reset” signal is generated. These two signals are then transmitted to the high-side by the level-shifting circuit and are input to the SR flip-flop circuit. Finally, the SR flip-flop circuit feeds an output signal, Q (i.e., HOx).

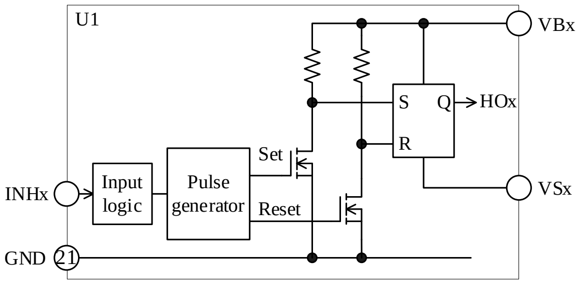


Figure 13-2. Internal Level-shifting Circuit

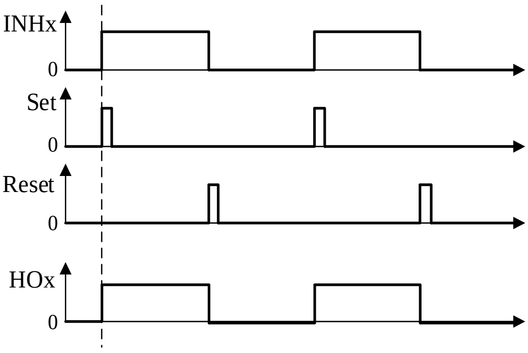


Figure 13-3. Operational Waveforms of Level-shifting Circuit

13.2.5. VSU, VSV, and VSW

These pins are the grounds of the high-side floating power supplies for each phase, and are connected to the negative nodes of bootstrap capacitors, $C_{BS1(X)}$ and $C_{BS2(X)}$. The VSU, VSV, and VSW pins are internally connected to the U, V, and W pins, respectively.

13.2.6. VCCHU, VCCHV, VCCHW, and VCCL

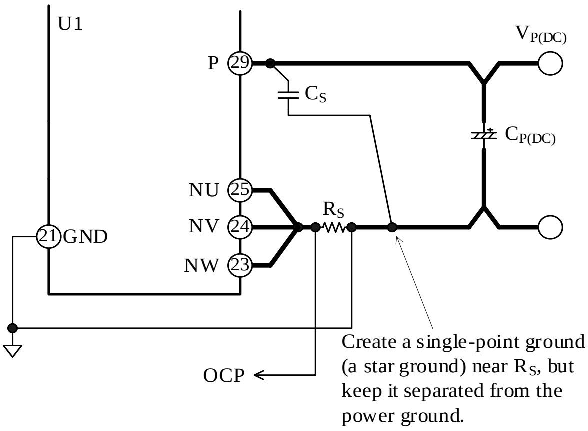
The VCCHU, VCCHV, and VCCHW pins are the power supply pins for the built-in high-side control MICs. The VCCL pin is the power supply pin for the built-in low-side control MIC. The VCCHx and VCCL pins must be externally connected on a PCB because they are not internally connected. To prevent malfunction induced by supply ripples or other factors, connect a capacitor of ≥22 µF (C_{VCC1}) and a capacitor of 0.47 µF to 2.2 µF ($C_{VCC2(L)}$) between the VCCL and GND pins with a minimal length of traces. In addition, connect a capacitor of 0.47 µF to 2.2 µF ($C_{VCC2(Hx)}$) between the VCCHx and GND pins with a minimal length of traces.

To prevent damage caused by surge voltages, put a 16.5 V to 20 V Zener diode, D_{VCC}, between the VCCL and GND pins.

Voltage to be applied between the VCCHx and GND pins should be regulated within the recommended operational range of V_{VCCHx}, given in Section 3. Voltage to be applied between the VCCL and GND pins should be regulated within the recommended operational range of V_{VCCL}, given in Section 3.

13.2.7. GND

This is the logic ground pins for the IC. For proper control, the control parts of the IC must be connected to the GND pin. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect the logic ground as close and short as possible to a shunt resistor, R_S, at a single-point ground (or star ground) which is separated from the power ground (see Figure 13-4). Moreover, extreme care should be taken in designing a PCB so that currents from the power ground do not affect the GND pin.



Create a single-point ground (a star ground) near R_S, but keep it separated from the power ground.

Figure 13-4. Connections to Logic Ground

13.2.8. INHU, INHV, and INHW; INLU, INLV, and INLW

These are the input pins of the internal motor drivers for each phase. The INHx pin acts as a high-side controller; the INLx pin acts as a low-side controller. Figure 13-5 shows an internal circuit diagram of the INHx or INLx pin. This is a comparator circuit with a built-in pull-down resistor.

Input signals across the INHx–GND and the INLx–GND pins in each phase should be set within the ranges provided in Table 13-1, below. Note that dead time setting must be done for INHx and INLx signals because the IC does not have a dead time generator.

The higher PWM carrier frequency rises, the more switching loss increases. Hence, the PWM carrier frequency must be set so that operational case temperatures and junction temperatures have sufficient margins against the absolute maximum ranges, specified in Section 2.

If the signals from the microcontroller become unstable, the IC may result in malfunctions. To avoid such malfunctions, set the microcontroller output line not to have high-impedance outputs. Also, if the traces from the microcontroller to the INHx or INLx pin (or both) are too long, the traces may be interfered by noise. Therefore, it is recommended to add an additional filter or a pull-down resistor near the INHx or INLx pin as needed (see Figure 13-6).

Here are filter circuit constants for reference:
R_{INH1x}, R_{INL1x}: 47 Ω to 220 Ω
R_{INH2x}, R_{INL2x}: 1 kΩ to 10 kΩ
C_{INHx}, C_{INLx}: 100 pF to 1500 pF

Care should be taken in adding R_{INH1x}, R_{INL1x}, R_{INH2x}, and R_{INL2x} to the traces. When they are connected to each other, the input voltage of the INHx and INLx pins becomes slightly lower than the output voltage of the microcontroller.

Table 13-1. Input Signals for INHx and INLx Pins

Parameter	High Level Signal	Low Level Signal
Input Voltage	$3\ V < V_{IN} < 5\ V$	$0\ V < V_{IN} < 0.5\ V$
Input Pulse Width	≥1.5 μs	≥1.5 μs
PWM Carrier Frequency	$5\ kHz \le f_{SW} \le 20\ kHz$	
Dead Time	≥1.5 μs	

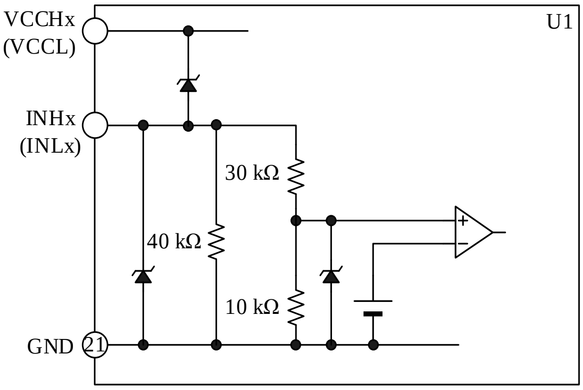


Figure 13-5. Internal Circuit Diagram of INHx or INLx Pin

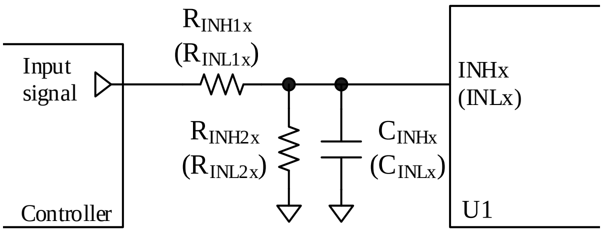


Figure 13-6. Filter Circuit for INHx or INLx Pin

13.2.9. OCP

This pin serves as the input of the overcurrent protection (OCP) which monitors the currents flowing through the low-side output transistors. Section 13.3.4 provides further information about the OCP circuit configuration and its mechanism.

13.2.10. CFO

The CFO pin determines the FO Pin OCP Hold Time,

t_{FO}, during the overcurrent protection (OCP) operation. To set t_{FO}, connect a capacitor, C_{CFO}, between the CFO and GND pins. Figure 13-7 shows how the OCP hold time, t_{FO}, and the capacitor, C_{CFO}, are related. C_{CFO} should have a capacitance of 0.01 μF to 1 μF.

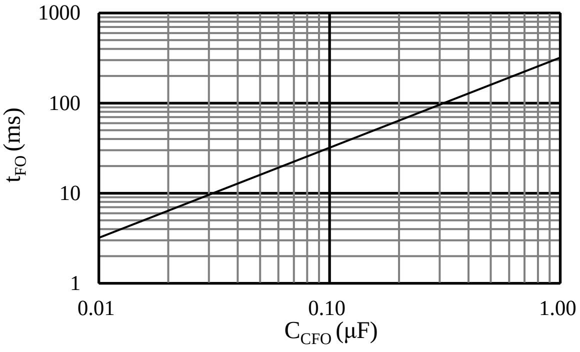


Figure 13-7. CFO Pin Capacitor, C_{CFO} vs. FO Pin OCP Hold Time, t_{FO}

13.2.11. FO

This pin operates as the fault signal output and the shutdown signal input. Sections 13.3.1 and 13.3.2 explain the two functions in detail, respectively.

Figure 13-8 illustrates an internal circuit diagram of the FO pin and its peripheral circuit. Because of its open-collector nature, the FO pin should be tied by a pull-up resistor, R_{FO}, to the external power supply. The external power supply voltage (i.e., the FO Pin Pull-up Voltage, V_{FO_PU}) should range from 3.0 V to 5.5 V. Therefore, it is recommended to use a 5.5 kΩ to 33 kΩ pull-up resistor.

To suppress noise, add a filter capacitor, C_{FO}, near the IC with minimizing a trace length between the FO and GND pins. The value of C_{FO} must be set to ≤3300 pF.

For avoiding repeated OCP activations, the external microcontroller must shut off any input signals to the IC within a fixed hold time, t_{FO}, after the internal MOSFET (Q_{FO}) turn-on. t_{FO} is the value where minimum values of thermal characteristics are taken into account (for more details, see Section 13.3.4).

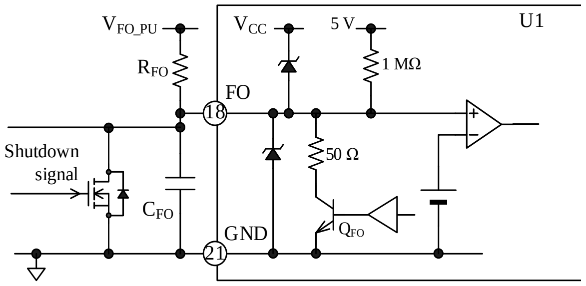


Figure 13-8. Internal Circuit Diagram of FO Pin and Its Peripheral Circuit

13.2.12. TH

The SAM265Mx0AA1 series incorporates a thermistor which monitors the temperatures inside the IC.

Figure 13-9 illustrates an internal circuit diagram of the TH pin and its peripheral circuit. The both ends of the internal thermistor are connected to the TH and GND pins, respectively.

Connect a noise filter capacitor, C_{TH}, between the TH and GND pins. C_{TH} should have a capacitance of ≥0.1 μF. Then, place C_{TH} as close as possible to the IC, and connect it between the pin connected to the microcontroller and the TH pin with minimizing respective trace lengths.

In addition, connect the external power supply, V_{TH_PU}, and the resistor, R_{TH}, to the TH pin. The external power supply, V_{TH_PU}, should have voltages ranging from 3.0 V to 5.5 V. Table 13-2 provides the recommended values for R_{TH} according to the external power supply.

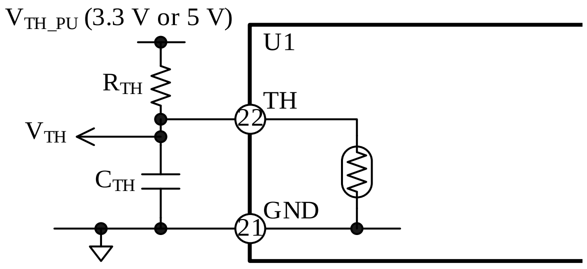


Figure 13-9. Internal Circuit Diagram of TH Pin and Its Peripheral Circuit

Table 13-2. Recommended R_{TH} Values

V_{TH_PU} (V)	R_{TH} (kΩ)		
	Min.	Typ.	Max.
3.3	6.8	15	33
5.0	10	22	47

The following figures show the relationships between the V_{TH} voltage and the thermistor temperature when V_{TH_PU} = 3.3 V (Figure 13-10) and when V_{TH_PU} = 5.0 V (Figure 13-11). Be sure to set the external power supply, V_{TH_PU}, and the resistor, R_{TH}, according to the thermistor temperature to be detected.

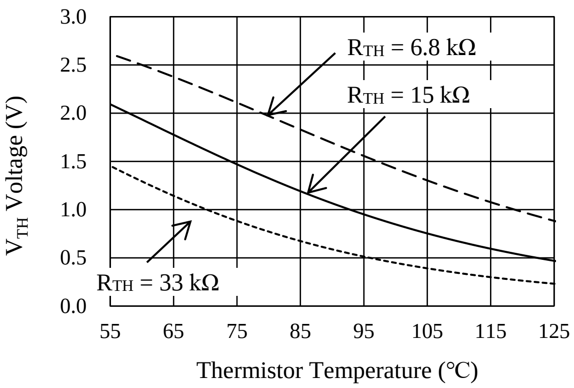


Figure 13-10. V_{TH} Voltage vs. Thermistor Temperature (V_{TH_PU} = 3.3 V)

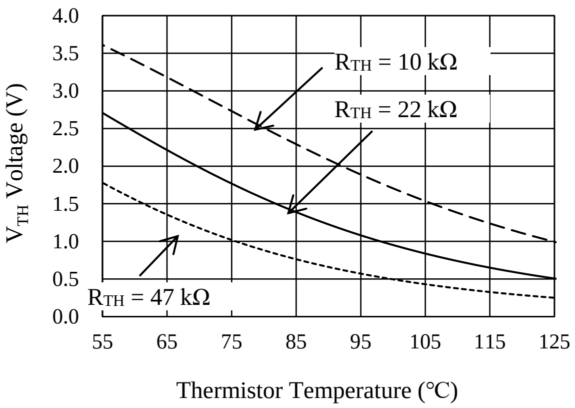


Figure 13-11. V_{TH} Voltage vs. Thermistor Temperature (V_{TH_PU} = 5.0 V)

The SAM265Mx0AA1 series does not have any protection against overtemperature; therefore, the motor must be externally controlled when a temperature rise occurs, or be controlled with such protective measures. Moreover, note that the TH pin output does not provide the temperature followability, especially when a rapid temperature rise in the output transistors occurs during motor lock and short circuit conditions.

13.3. Protection Functions

This section describes the various protection circuits provided in the SAM265Mx0AA1 series. The protection circuits include the VBx pin undervoltage lockout for power supply (UVLO_VBx), the VCCL pin undervoltage lockout for power supply (UVLO_VCCL), and the overcurrent protection (OCP).

In case the UVLO_VCCL or OCP circuit is activated, the FO pin outputs a fault signal; as a result, the external microcontroller can stop the operations of the three phases by receiving the fault signal. The external microcontroller can also shut down IC operations by inputting a fault signal to the FO pin.

13.3.1. Fault Signal Output

In case one or more of the following protections are actuated, an internal transistor, Q_{FO}, turns on, then the FO pin becomes logic low (0.09 V).

1) VCCL pin undervoltage lockout for power supply (UVLO_VCCL)
2) Overcurrent protection (OCP)

While the FO pin is in the low state, all the low-side transistors turn off. In normal operation, the FO pin outputs a high signal of about 5 V. The FO Pin OCP Hold Time, t_{FO}, is determined by a value of the capacitor, C_{CFO}, connected to the CFO pin (see Section 13.2.10).

For avoiding repeated OCP activations, the external microcontroller must shut off any input signals to the IC within a fixed hold time, t_{FO}, after the internal MOSFET (Q_{FO}) turn-on. t_{FO} is the value where minimum values of thermal characteristics are taken into account (for more details, see Section 13.3.4).

13.3.2. Shutdown Signal Input

The FO pin also acts as the input pin of shutdown signals. When the FO pin becomes logic low, all the low-side transistors turn off. The voltages and pulse widths of shutdown signals should be set as listed in Table 13-3.

Table 13-3. Shutdown Signals

Parameter	High Level Signal	Low Level Signal
FO Pin Voltage	3 V < V_{FO} < 5.5 V	0 V < V_{FO} < 0.5 V
Input Pulse Width	≥3.0 μs	≥3.0 μs

When the FO pin becomes logic high, all the low-side transistors operate according to input signals to the INLx pin. The FO pin has an internal filter circuit of 2.5 μs to prevent noise-induced malfunctions.

Figure 13-12 shows the operational waveforms at shutdown signal input. Figure 13-13 illustrates an internal circuit diagram of the FO pin and its peripheral circuit.

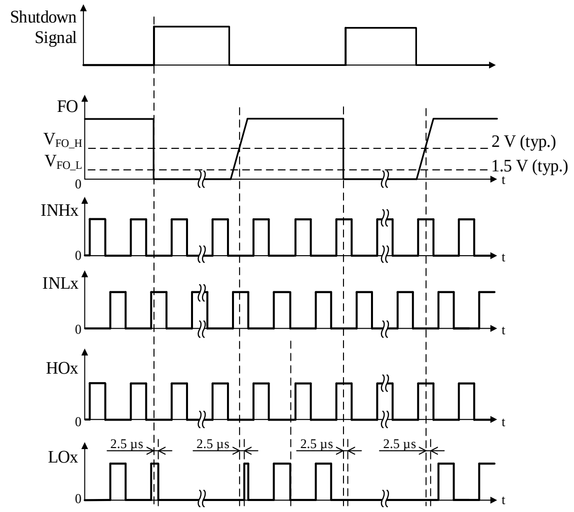


Figure 13-12. Operational Waveforms at Shutdown Signal Input

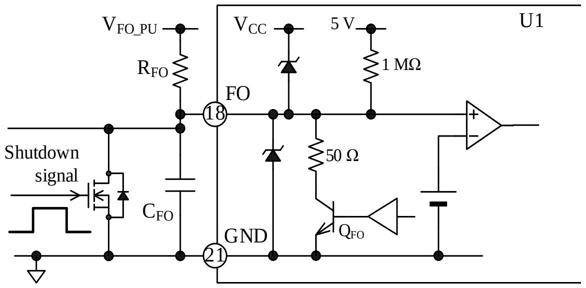


Figure 13-13. Internal Circuit Diagram of FO Pin and Its Peripheral Circuit

13.3.3. Undervoltage Lockout for Power Supply (UVLO)

In case the gate-driving voltages of the output transistors decrease, their steady-state power dissipations increase. This overheating condition may cause permanent damage to the IC in the worst case. To prevent this event, the IC has the undervoltage lockout (UVLO) circuits for each of the VBx and VCCL pins.

13.3.3.1. VBx Pin Undervoltage Lockout (UVLO_VBx)

Figure 13-14 shows operational waveforms of the VBx pin undervoltage lockout for power supply (i.e., UVLO_VBx).

When the voltage between the VBx and VSx pins (VBx–VSx) decreases to $V_{\mathrm{VBx\text{-}VSx\_L}}$ = 11.6 V or less, the UVLO_VBx circuit in the corresponding phase gets activated and sets an HOx signal to logic low.

When the voltage between the VBx and VSx pins increases to $V_{\mathrm{VBx\text{-}VSx\_H}}$ = 12.1 V or more, the IC releases the UVLO_VBx condition. Then, the HOx signal becomes logic high at the rising edge of the first input command after the UVLO_VBx release.

Any fault signals are not output from the FO pin during the UVLO_VBx operation. The VBx pin has an internal filter circuit of about 1.8 μs to prevent noise-induced malfunctions.

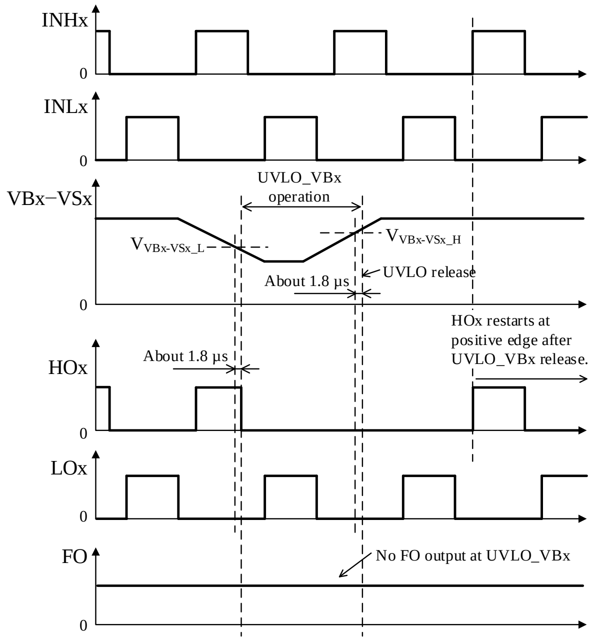


Figure 13-14. UVLO_VBx Operational Waveforms

13.3.3.2. VCCL Pin Undervoltage Lockout (UVLO_VCCL)

Figure 13-15 shows operational waveforms of the VCCL pin undervoltage lockout for power supply (i.e., UVLO_VCCL).

When the VCCL pin voltage decreases to $V_{\mathrm{VCCL\_L}}$ = 12.1 V or less, the UVLO_VCCL circuit gets activated and sets an LOx signal to logic low.

When the VCCL pin voltage increases to $V_{\mathrm{VCCL\_H}}$ = 12.6 V or more, the IC releases the UVLO_VCCL condition. Then it resumes transmitting the LOx signal according to an input command on the INLx pin.

During the UVLO_VCCL operation, the FO pin becomes logic low and sends fault signals. The VCCL pin has an internal filter circuit of about 1.8 μs to prevent noise-induced malfunctions.

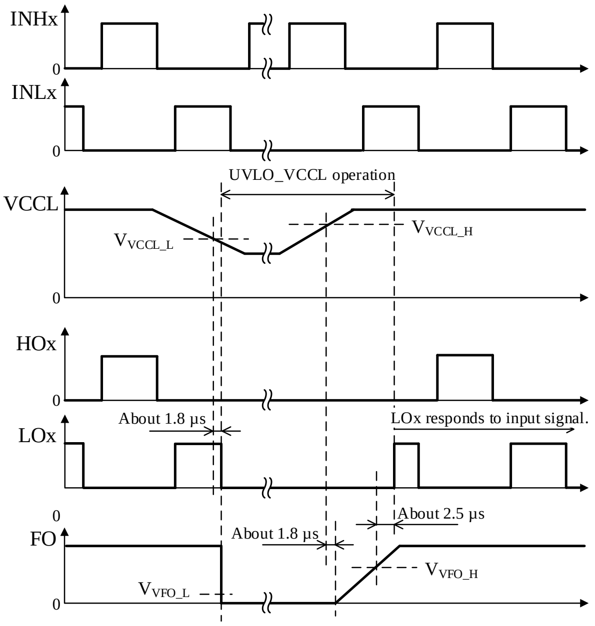


Figure 13-15. UVLO_VCCL Operational Waveforms

13.3.4. Overcurrent Protection (OCP)

The OCP pin has the overcurrent protection (OCP) circuit. Figure 13-16 is an internal circuit diagram describing the OCP pin and its peripheral circuit.

The OCP pin detects overcurrents with voltage across an external shunt resistor, R_S. Because the OCP pin is internally pulled down, the OCP pin voltage increases proportionally to a rise in the current running through the shunt resistor, R_S.

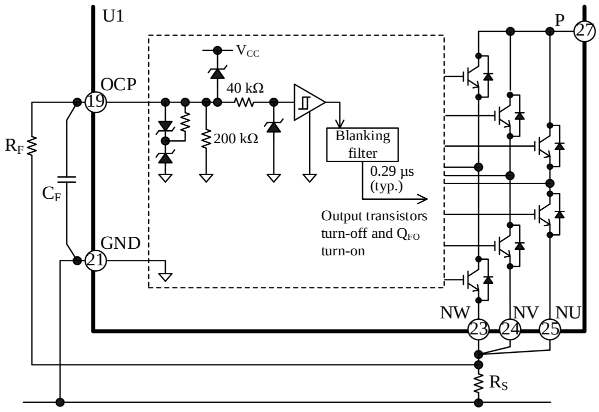


Figure 13-16. Internal Circuit Diagram of OCP Pin and Its Peripheral Circuit

Figure 13-17 shows operational waveforms when the OCP pin detects an overcurrent condition. When the OCP pin voltage increases to V_{OCP_H} = 0.50 V or more, and remains in this condition for 0.29 µs or longer, the OCP circuit is activated. When the OCP is activated, the IC puts an LOx signal and the FO pin to logic low. The low-side transistors turn off as the LOx signal becomes logic low; as a result, output current decreases. Even if the OCP pin voltage falls below V_{OCP_L}, the IC holds the FO pin in the low state for a fixed OCP hold time (t_{FO}). The low-side transistors also remain turned off during this period. Then, the output transistors operate according to input signals.

The OCP pin has an internal filter circuit of about 0.29 µs to prevent noise-induced malfunctions.

The FO Pin OCP Hold Time, t_{FO}, is determined by a value of the capacitor, C_{CFO}, connected to the CFO pin (see Section 13.2.10).

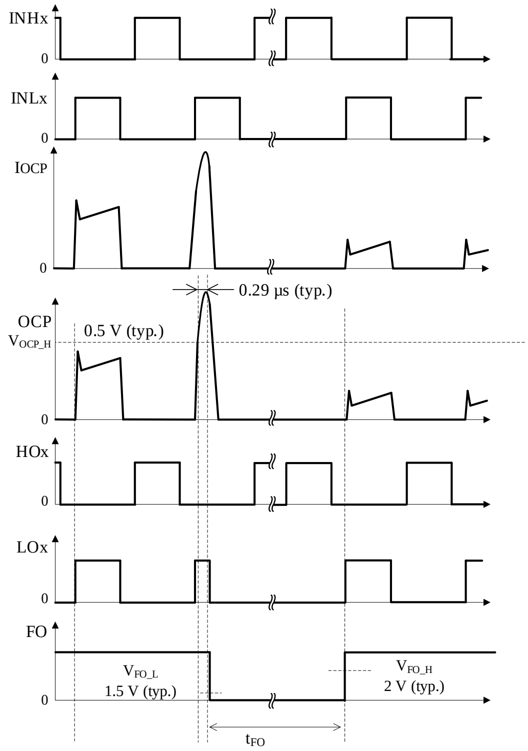


Figure 13-17. OCP Operational Waveforms

The OCP is used for detecting abnormal conditions, such as an output transistor shorted. In case short-circuit conditions occur repeatedly, the output transistors can be destroyed. For this reason, motor operations must be controlled by the external microcontroller so that it can immediately stop the motor when fault signals are detected.

The external microcontroller receives the fault signals with its interrupt pin (INT), and must be programmed to put the INHx and INLx pins to logic low within a predetermined OCP hold time, t_{FO}. To resume the motor operation thereafter, set the motor to be resumed after a lapse of ≥2 seconds.

For proper shunt resistor setting, your application must meet the following:

- Use the shunt resistor that has a recommended resistance, R_S (see Section 3).
- Set the OCP pin input voltage to vary within the rated OCP pin voltages, V_{OCP} (see Section 2).
- Keep the current through the output transistors below the rated collector current (peak), I_{CP} (see Section 2).
- Surface-mount current detection resistor
- Allowable tolerance: ±2% or less
- Thermal coefficient: ±200 ppm/°C or less

It is required to use a resistor with low internal inductance because high-frequency switching current will flow through the shunt resistor, R_S. In addition, choose a resistor with allowable power dissipation according to your application.

When you connect a CR filter (i.e., a pair of a filter resistor, R_F, and a filter capacitor, C_F) to the OCP pin, care should be taken in setting the time constants of R_F and C_F. The larger the time constant, the longer the time that the OCP pin voltage rises to V_{OCP_H}. And this may cause permanent damage to the transistors. Be sure to set the time constants of R_F and C_F to 1.5 µs or less so that the OCP can start to operate within 2.0 µs when a short circuit condition occurs. And place C_F as close as possible to the IC with minimizing a trace length between the OCP and GND pins.

Note that overcurrents are undetectable when one or more of the U, V, and W pins or their traces are shorted to ground (ground fault). In case any of these pins falls into a state of ground fault, the output transistors may be destroyed.

14. Design Notes

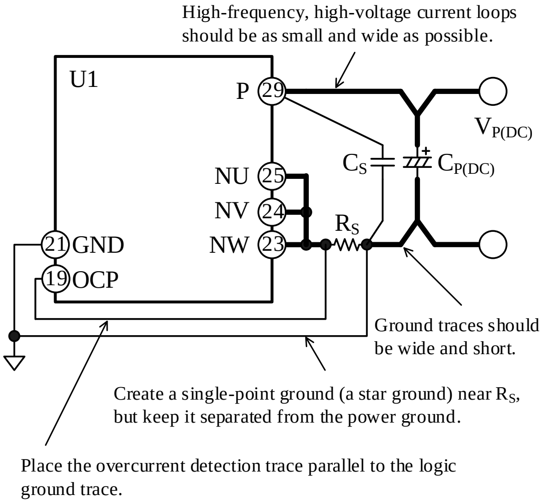
14.1. PCB Pattern Layout

Figure 14-1 shows a schematic diagram of a motor driver circuit. The motor driver circuit consists of current paths having high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing. Current loops (especially, between the P pin, $C_{P(DC)}$, and the Nx pin) should be as small and wide as possible, in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

A shunt resistor, R_S, should be placed as close as possible to the IC with minimizing a trace length between the Nx pin and a capacitor, $C_{P(DC)}$.

Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect the logic ground as close and short as possible to the shunt resistor, R_S, at a single-point ground (or star ground) which is separated from the power ground (see Figure 14-1). Moreover, extreme care should be taken when wiring so that currents from the power ground do not affect the logic ground (e.g., the control ground trace is not placed parallel near the power ground, and these traces are not crossed as much as possible).

To reduce the noise effect to the OCP pin, connect the overcurrent detection trace as near as possible to the shunt resistor, R_S (see Figure 14-1 and Figure 14-2). Also, place the overcurrent detection trace parallel to the logic ground trace and connect it to the OCP pin.



High-frequency, high-voltage current loops should be as small and wide as possible.

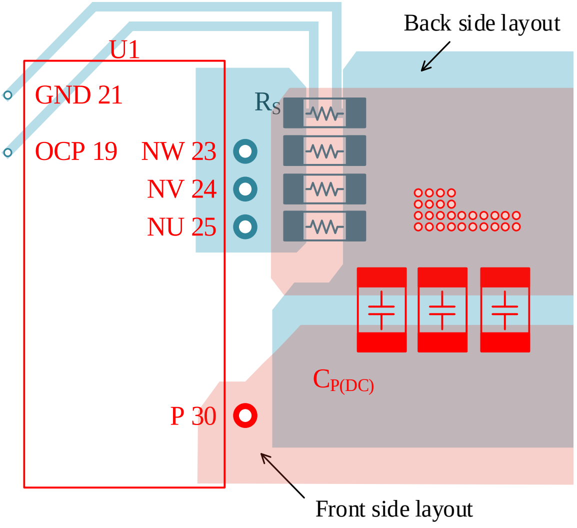
Ground traces should be wide and short.

Create a single-point ground (a star ground) near R_S, but keep it separated from the power ground.

Place the overcurrent detection trace parallel to the logic ground trace.

Figure 14-1. High-frequency and High-voltage Current Paths, and Connections to Logic Ground

To reduce noises generated by electromagnetic induction by high-frequency current, use a double-sided board to offset the magnetic field. For example, as shown in Figure 14-2, design the trace from the P pin to $C_{P(DC)}$ on the front side, and the trace from $C_{P(DC)}$ to the Nx pin on the back side. Then, overlap these traces. The currents flowing from the P pin to $C_{P(DC)}$, and from $C_{P(DC)}$ to the Nx pin are the same value. Thus, overlapping these traces so that their current directions are opposite offsets the generated magnetic field, and reduces the noises.



Back side layout

Front side layout

Figure 14-2. Peripheral Layout Example of $C_{P(DC)}$ (Double-sided Board)

14.2. Considerations in Heatsink Mounting

The following are the key considerations and the guidelines for mounting a heatsink:

- Be sure to use a metric screw of M3 and a plain washer of 7 mm (φ). To tighten the screws, use a torque screwdriver. Tighten the two screws firstly up to 20% to 30% of the maximum screw torque, then finally up to 100% of the prescribed maximum screw torque. Perform appropriate tightening within the range of screw torque defined in Section 5. The order of the screws does not matter to the temporary tightening. Note that the sequence when the screws are tightened finally must be the same order as these are tightened firstly.
- When mounting a heatsink, it is recommended to use silicone greases. If a thermally conductive sheet or an electrically insulating sheet is used, package cracks may be occurred due to creases at screw tightening. Therefore, you should conduct thorough evaluations before using these materials.
- When applying a silicone grease, make sure that there are no foreign substances between the IC and a heatsink. Extreme care should be taken not to apply a

silicone grease onto any device pins as much as possible. The following requirements must be met for proper grease application:

– Grease thickness: 100 µm to 200 µm

14.3. Considerations in IC Characteristics Measurement

When checking the characteristics of the internal switching elements (IGBTs and freewheeling diodes), the IGBTs may result in permanent damage unless these are measured appropriately. Therefore, the following should be taken into account. The absolute maximum rating of the Collector-to-Emitter Voltage, V_{CES}, is 650 V.

- Do not measure the withstand voltage of the internal IGBTs. Applying the voltage of V_{CES} or more between the collector and emitter may degrade the IGBTs.
- Measurement condition of the leakage current of the internal IGBTs must be below V_{CES}.
- The leakage current value is the total leakage current of such as IGBT, freewheeling diode, control IC, and bootstrap diode. These leakage currents can not be measured individually.
- When measuring leakage current of the IGBTs, note that the gate and emitter of the IGBT must be the same potential. The gate of the high-side IGBT is pulled down to the emitter inside the IC, but the gate of the low-side IGBT is pulled down to the COM pin inside the IC. To prevent damage of the IGBTs, the Nx and COM pins shoud be shorted and measured.

The following are circuit diagrams representing typical measurement circuits for breakdown voltage: Figure 14-3 shows the high-side IGBT (Q_{LH}) in the U-phase; Figure 14-4 shows the low-side IGBT (Q_{LU}) in the U-phase.

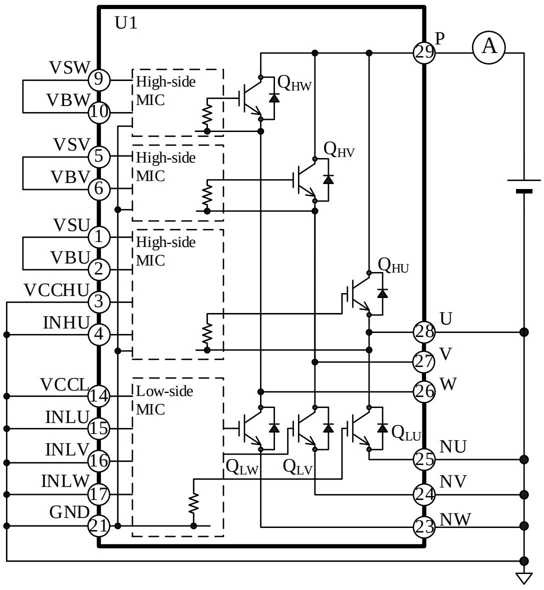


Figure 14-3. Typical Leakage Current Measurement Circuit for High-side IGBT (Q_{HU}) in U-phase

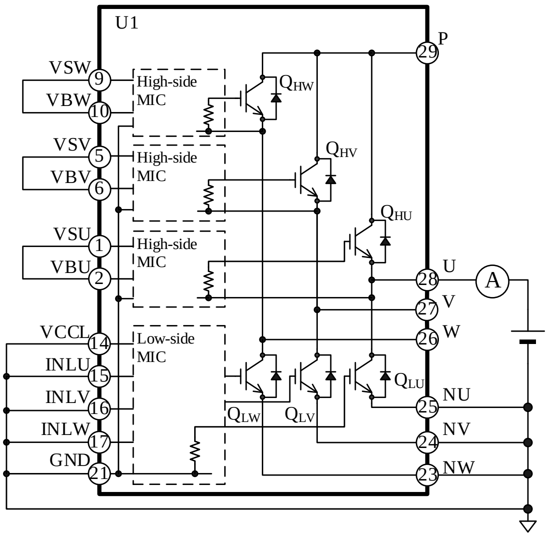


Figure 14-4. Typical Leakage Current Measurement Circuit for Low-side IGBT (Q_{LU}) in U-phase

15. Calculating Power Losses and Estimating Junction Temperature

This section describes the procedures to calculate power losses in a switching transistor, and to estimate a junction temperature. Note that the descriptions listed here are applicable to the SAM265Mx0AA1 series, which is controlled by a 3-phase sine-wave PWM driving strategy.

Total power loss in an IGBT can be obtained by taking the sum of steady-state loss, P_{ON}, and switching loss, P_{SW}. The following subsections contain the mathematical procedures to calculate the power losses in an IGBT and its junction temperature.

For quick and easy references, we offer calculation support tools online. Please visit our website to find out more.

- DT0076: SAM265Mx0AA1 Calculation Tool
  https://www.semicon.sanken-ele.co.jp/en/calc-tool/igbt1_caltool_automotive_en.html

15.1. IGBT Steady-state Loss, P_{ON}

Figure 15-1 shows the linear approximation ($V_{CE(SAT)} = \alpha \times I_C + \beta$) based on the $V_{CE(SAT)}$ vs. I_C curve at a range the I_C is actually used.

The values gained by the above calculation are then applied as parameters in Equation (4), below. Hence, the equation to obtain the IGBT steady-state loss, P_{ON}, is:

$$P_{ON} = \frac{1}{2\pi}\int_0^{\pi} V_{CE(SAT)}(\varphi) \times I_C(\varphi) \times DT \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2}+\frac{4}{3\pi}M\times\cos\theta\right)I_M{}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2}+\frac{\pi}{8}M\times\cos\theta\right)I_M . \qquad (4)$$

Where:

$V_{CE(SAT)}$ is the collector-to-emitter saturation voltage of the IGBT (V),
I_C is the collector current of the IGBT (A),
DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),
cosθ is the motor power factor (0 to 1),
I_M is the effective motor current (A),
α is the slope of the linear approximation in the $V_{CE(SAT)}$ vs. I_C curve, and
β is the intercept of the linear approximation in the $V_{CE(SAT)}$ vs. I_C curve.

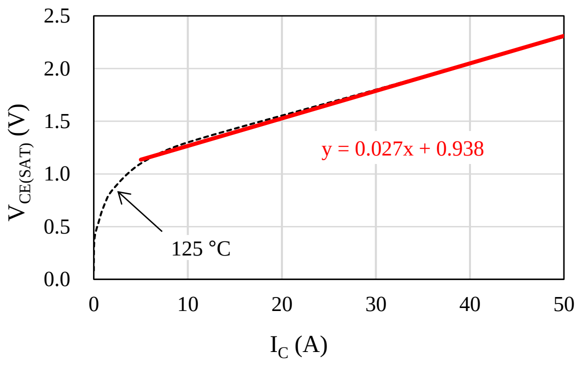


Figure 15-1. Linear Approximate Equation of $V_{CE(SAT)}$ vs. I_C

15.2. IGBT Switching Loss, P_{SW}

Switching loss in an IGBT, P_{SW}, can be calculated by Equation (5), letting I_M be the effective current value of the motor:

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{P(DC)}}{300} . \qquad (5)$$

Where:

f_C is the PWM carrier frequency (Hz),
$V_{P(DC)}$ is the main power supply voltage (V), i.e., the P pin input voltage, and
α_E is the slope of the switching loss curve (see Section 16.2.2).

15.3. Estimating Junction Temperature of IGBT

The junction temperature of an IGBT, T_J, can be estimated with Equation (6):

$$T_J = R_{(J-C)Q} \times (P_{ON} + P_{SW}) + T_C . \qquad (6)$$

Where:

$R_{(J-C)Q}$ is the junction-to-case thermal resistance per IGBT (°C/W), and
T_C is the case temperature (°C), measured at the point defined in Section 4.4.

16. Performance Curves

16.1. Transient Thermal Resistance Curves

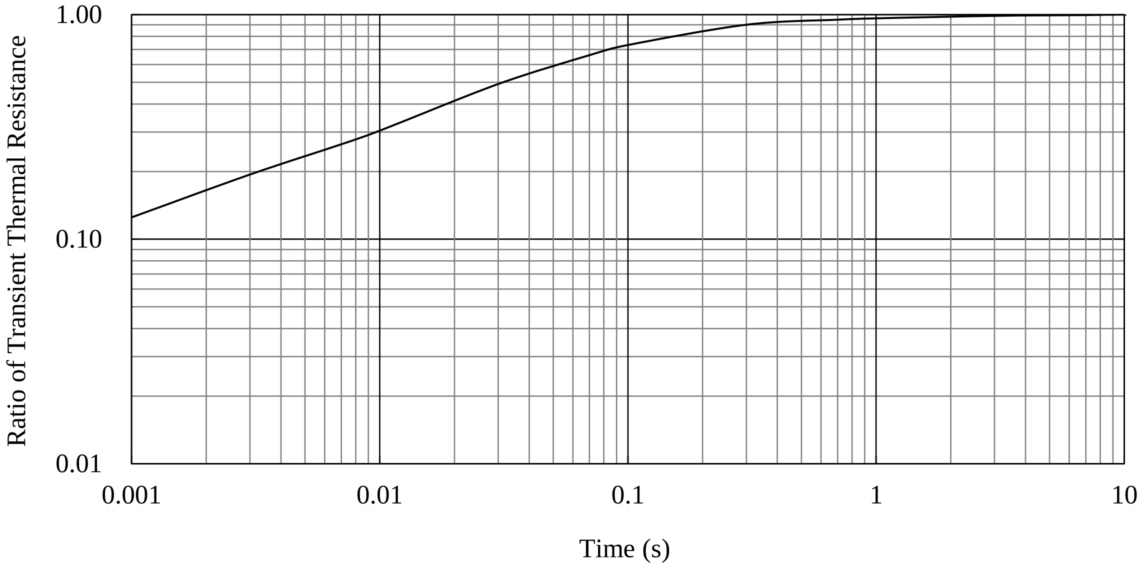


Figure 16-1. Transient Thermal Resistance: SAM265M30AA1

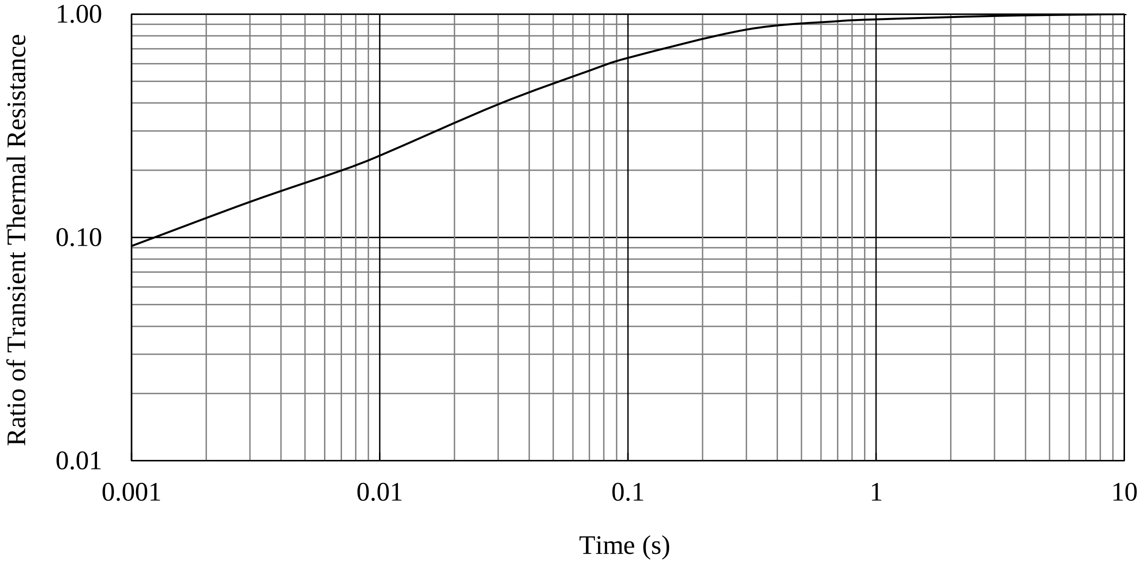


Figure 16-2. Transient Thermal Resistance: SAM265M50AA1

16.2. Performance Curves of Output Parts

16.2.1. Output Transistor Performance Curves

16.2.1.1. SAM265M30AA1

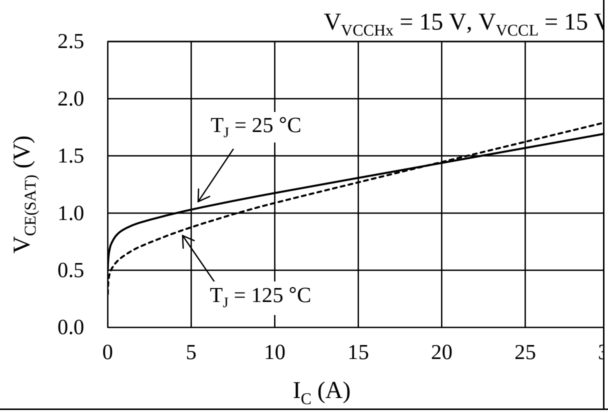


Figure 16-3. IGBT $V_{CE(SAT)}$ vs. I_C

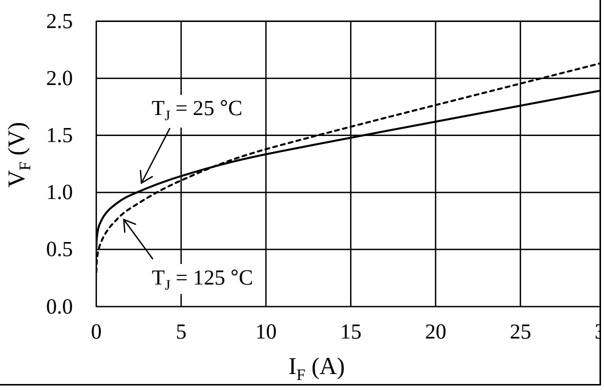


Figure 16-4. Freewheeling Diode V_F vs. I_F

16.2.1.2. SAM265M50AA1

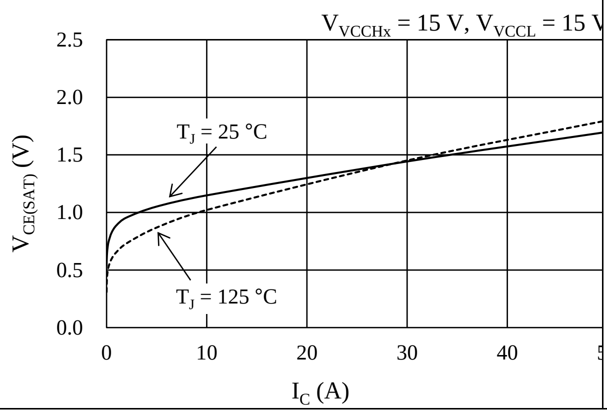


Figure 16-5. IGBT $V_{CE(SAT)}$ vs. I_C

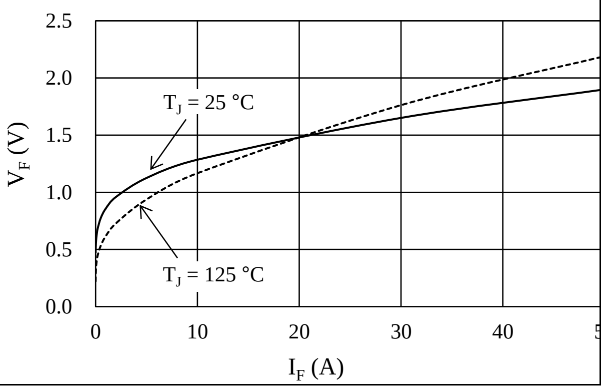


Figure 16-6. Freewheeling Diode V_F vs. I_F

16.2.2. Switching Loss Curves

Conditions: P pin voltage = 300 V, half-bridge circuit with inductive load.
Switching Loss, E, is the sum of turn-on loss and turn-off loss.

16.2.2.1. SAM265M30AA1

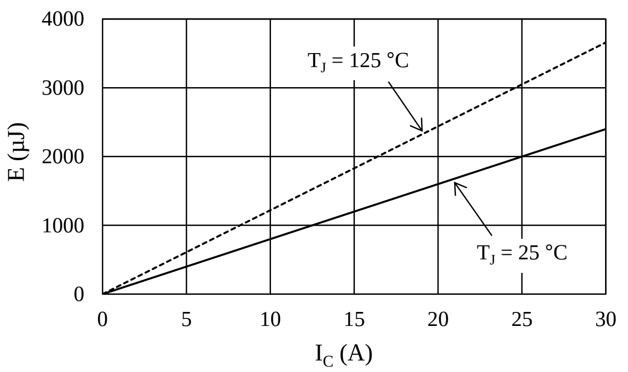


Figure 16-7. High-side Switching Loss

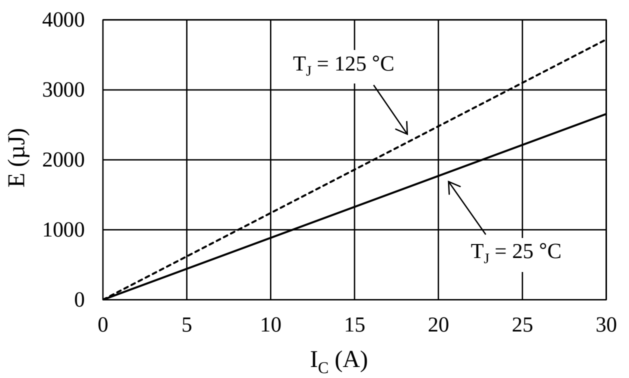


Figure 16-8. Low-side Switching Loss

16.2.2.2. SAM265M50AA1

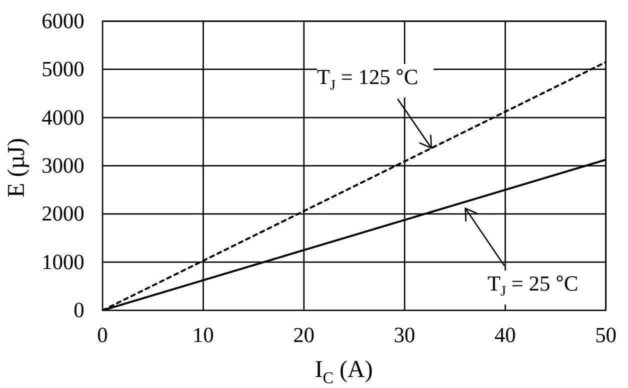


Figure 16-9. High-side Switching Loss

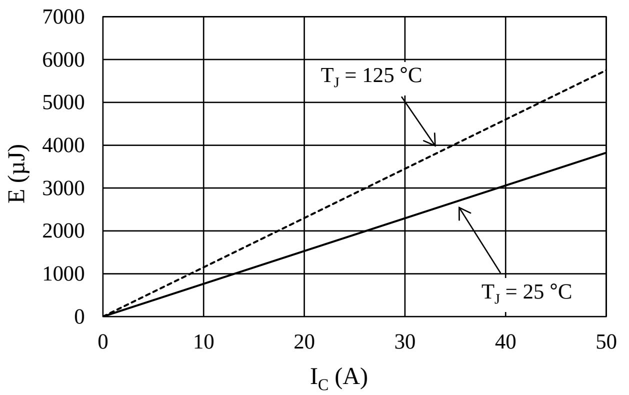


Figure 16-10. Low-side Switching Loss

16.3. Allowable Effective Current Curves

The following curves represent allowable effective currents in 3-phase sine-wave PWM driving with parameters such as maximum $V_{CE(SAT)}$ and maximum switching losses.

Operating conditions: P pin input voltage, $V_{P(DC)}$ = 300 V; VCCHx pin input voltage, V_{VCCHx} = 15 V; VCCL pin input voltage, V_{VCCL} = 15 V; modulation index, M = 1.0; junction temperature, T_J = 150 °C; output frequency = 60 Hz.

16.3.1. SAM265M30AA1

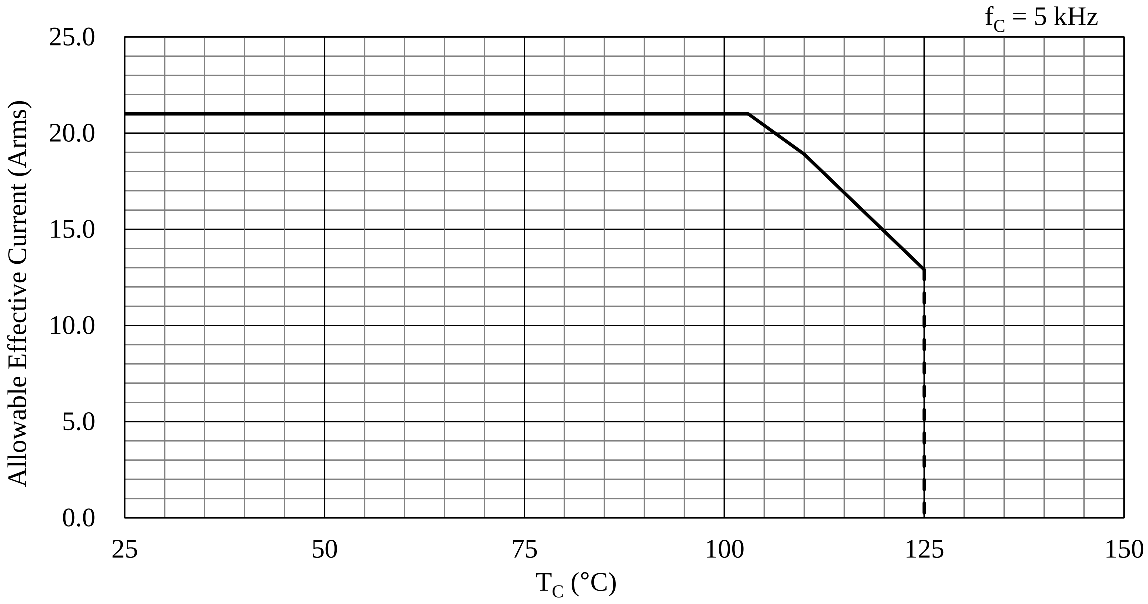


Figure 16-11. Allowable Effective Current (f_C = 5 kHz)

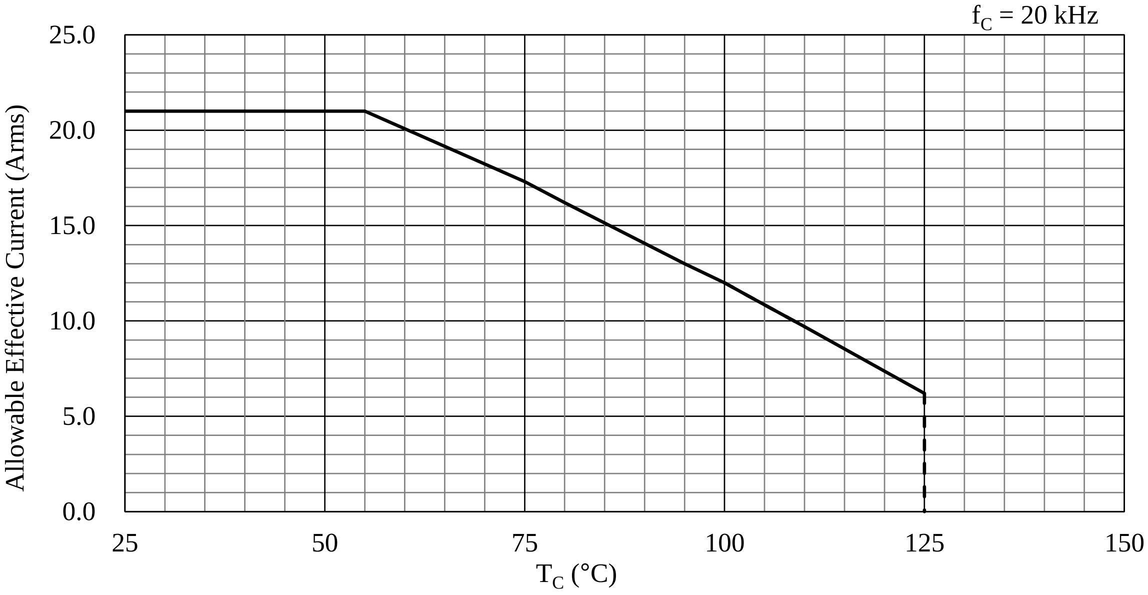


Figure 16-12. Allowable Effective Current (f_C = 20 kHz)

16.3.2. SAM265M50AA1

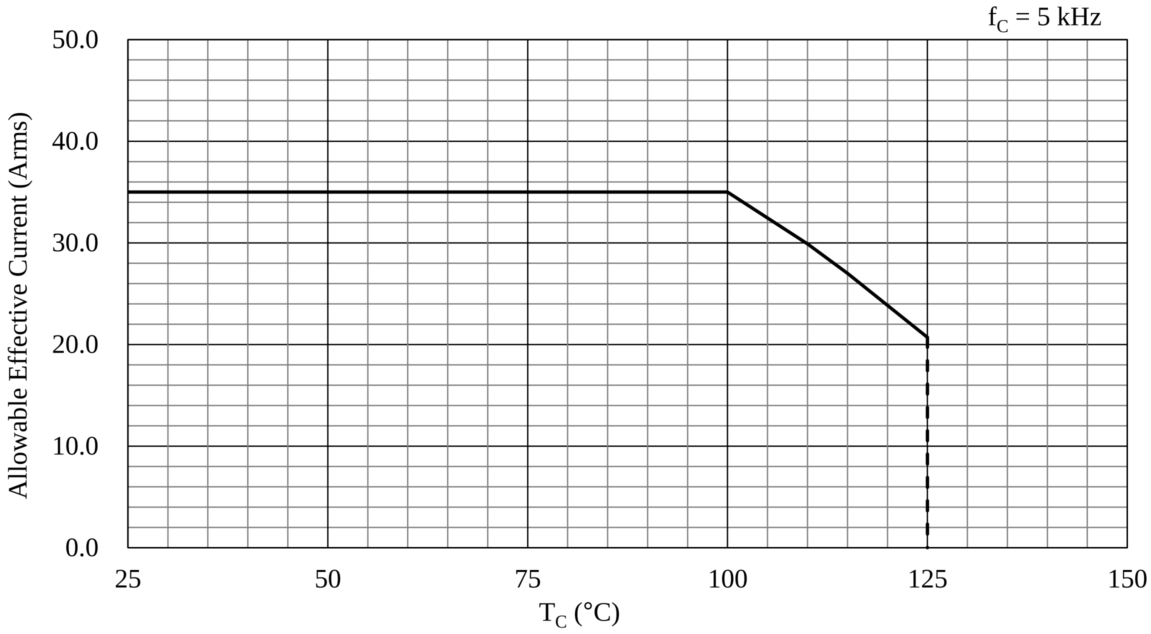


Figure 16-13. Allowable Effective Current (f_C = 5 kHz)

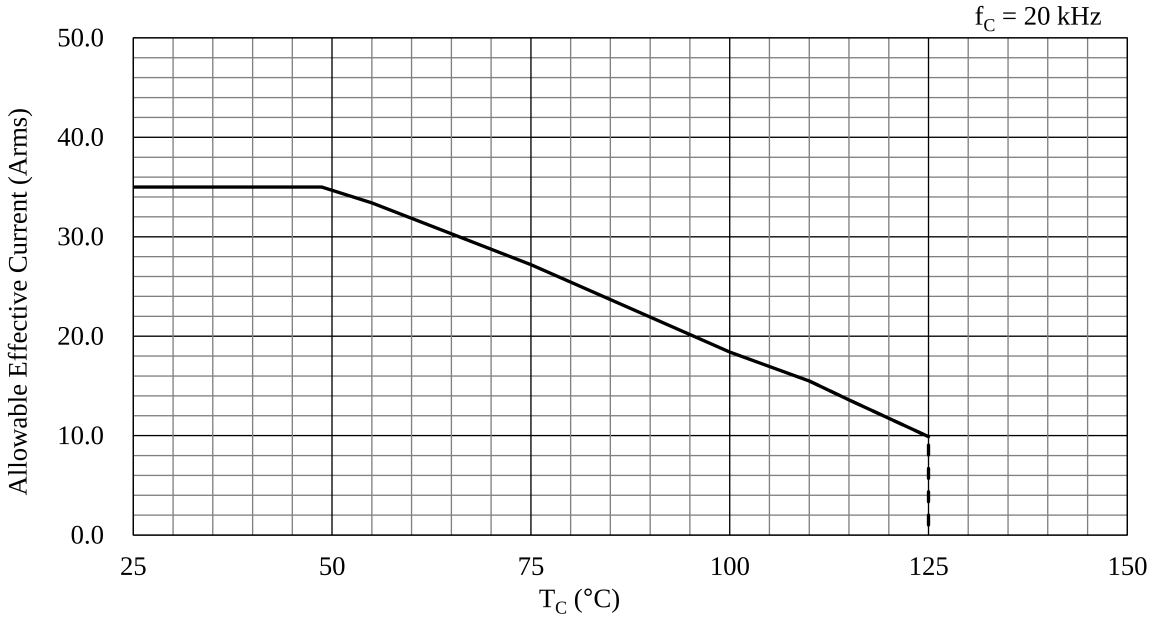


Figure 16-14. Allowable Effective Current (f_C = 20 kHz)

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DSGN-AEZ-16003