

**650 V, 50 A**  
**3-phase Motor Driver**  
**SAM265M50BS3**



**Data Sheet**

**Description**

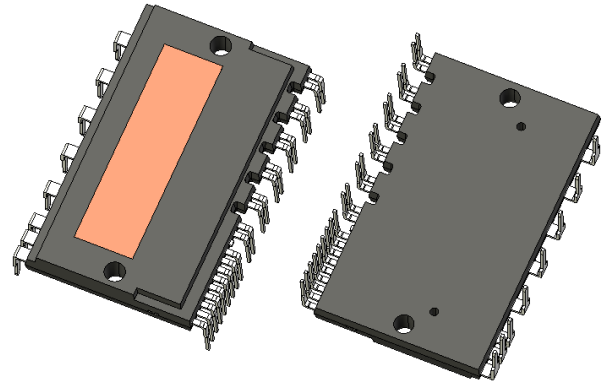
The SAM265M50BS3 is a 3-phase brushless motor driver in which output transistors, a pre-drive circuit, bootstrap diodes with current-limiting resistors, and a temperature-sensing thermistor are highly integrated. The IC is suitable for driving 3-phase motor of the units such as industrial equipment.

**Features**

- Pb-free (RoHS Compliant)
- Isolation Voltage: 2500 V (for 1 min)  
(UL-recognized Component)
- Built-in Thermistor
- Built-in Bootstrap Diodes
- CMOS-compatible Input (3.3 V or 5 V)
- Fault Signal Output at Protection Activation
- Shutdown Signal Input
- Adjustable OCP Hold Time
- Protection Functions
  - Undervoltage Lockout for Power Supply  
VBx Pin (UVLO\_VBx): Auto-restart  
VCCL Pin (UVLO\_VCCL): Auto-restart
  - Overcurrent Protection (OCP): Auto-restart

**Package**

DIP30 (Leadform: 2541)

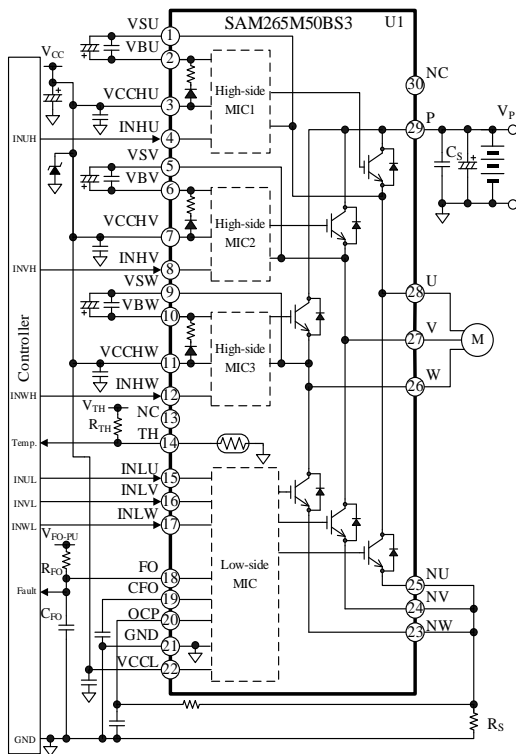


Not to scale

**Specifications**

- Breakdown Voltage: 650 V
- Output Current: 50 A

**Typical Application**



**Applications**

For driving 3-phase motors used in industrial equipment such as:

- Commercial Air Conditioner Compressor
- General-purpose Inverter

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**1. Introduction**

For pin descriptions, this document employs a notation system that denotes a pin name with the arbitrary letter “x”, depending on context. The U-, V-, and W-phase (3-phases) output pins are represented as the pin numbers U, V, and W, respectively. Thus, “the VBx pin” is used when referring to any or all of the VBU, VBV, and VBW pins. When different pin names are mentioned as a pair (e.g., “the VBx and VSx pins”), they are meant to be the pins in the same phase. Also, “the OUTx pin” is used when referring to any or all of the output pins (U, V, and W).

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (-).

**2. Absolute Maximum Ratings**

Unless specifically noted,  $T_A = 25\text{ }^\circ\text{C}$ .

Parameter	Symbol	Conditions	Ratings	Unit
<b>Inverter Stage</b>				
Main Supply Voltage (DC)	$V_{P(DC)}$	P-Nx	500	V
Main Supply Voltage (Surge)	$V_{P(SURGE)}$	P-Nx	550	V
Collector-to-Emitter Voltage (Surge)	$V_{CE(SURGE)}$	P-OUTx, OUTx-Nx	550	V
Collector-to-Emitter Voltage	$V_{CES}$	Built-in IGBT chip	650	V
Collector Current <sup>(1)</sup>	$I_C$	$T_C = 25\text{ }^\circ\text{C}$	50	A
Collector Current (Peak) Power Dissipation	$I_{CP}$	$T_C = 25\text{ }^\circ\text{C}$ , Pulse width < 1 ms, Duty cycle < 1%	100	A
Power Dissipation	$P_C$	$T_C = 25\text{ }^\circ\text{C}$ , 1 element operating (IGBT)	150	W
		$T_C = 25\text{ }^\circ\text{C}$ , 1 element operating (freewheeling diode)	75	W
<b>Control Parts</b>				
Nx Pin Voltage	$V_{Nx}$	Nx-GND	-5 to 5	V
VCCHx Pin Voltage	$V_{VCCHx}$	VCCHx-GND	-0.5 to 25	V
VCCL Pin Voltage	$V_{VCCL}$	VCCL-GND	-0.5 to 25	V
VBx-VSx Pin Voltage	$V_{VBx-VSx}$	VBx-VSx	-0.5 to 25	V
INHx Pin Voltage	$V_{INHx}$	INHx-GND	-0.5 to $V_{VCCHx} + 0.3$	V
INLx Pin Voltage	$V_{INLx}$	INLx-GND	-0.5 to $V_{VCCL} + 0.3$	V
FO Pin Voltage	$V_{FO}$	FO-GND	-0.5 to $V_{VCCL} + 0.3$	V
FO Pin Sink Current	$I_{FO}$		1	mA
OCP Pin Voltage	$V_{OCP}$	OCP-GND	-0.5 to $V_{VCCL} + 0.3$	V
Change Rate of VCC Supply Voltage Time	$\Delta V_{VCC}/\Delta t$		-1 to 1	V/ $\mu\text{s}$

<sup>(1)</sup> Should be derated depending on an actual case temperature.

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Parameter	Symbol	Conditions	Ratings	Unit
<b>Bootstrap Circuit</b>				
Bootstrap Diode Reverse Voltage	$V_{R-BS}$		650	V
<b>Thermistor</b>				
Operating Thermistor Temperature	$T_{TH}$		-40 to 150	°C
Thermistor Allowable Current	$I_{TH-MAX}$		1.8	mA
Thermistor Allowable Power	$P_{TH-MAX}$		200	mW
<b>Common</b>				
Junction Temperature	$T_J$	IGBTs and freewheeling diodes	-40 to 175	°C
		Control MICs	-40 to 150	°C
Operating Case Temperature <sup>(2)</sup>	$T_C$	For measurement point, see Figure 2-1.	-40 to 125	°C
Storage Temperature	$T_{STG}$		-40 to 150	°C
Isolation Voltage <sup>(3)</sup>	$V_{ISO(RMS)}$	Between surface of heatsink side and each pin; AC, 60 Hz, 1 min	2500	V

<sup>(2)</sup> Refers to a case temperature measured during IC operation.

<sup>(3)</sup> Refers to voltage conditions to be applied between all of the pins and the case. All the pins have to be shorted.

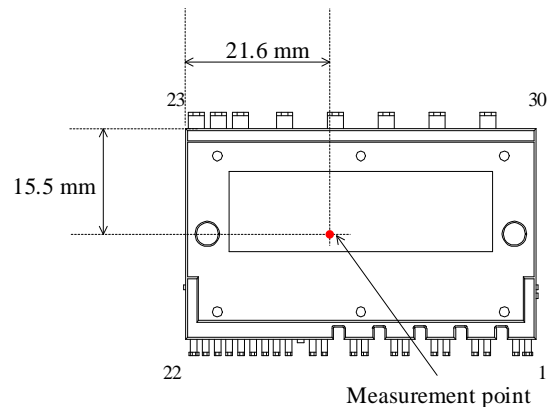


Figure 2-1. Case Temperature Measurement Point

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### 3. Recommended Operating Conditions

Unless specifically noted,  $T_C = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ ,  $V_{P(DC)} = 300\text{ V}$ ,  $V_{VCCHx} = V_{VCCL} = 15\text{ V}$ ,  $R_{FO} = 10\text{ k}\Omega$ ,  $C_{FO} = 0\text{ }\mu\text{F}$ ,  $V_{FO-PU} = 5\text{ V}$ .

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Main Supply Voltage (DC)	$V_{P(DC)}$	P–Nx	150	300	450	V
VCCHx Pin Voltage	$V_{VCCHx}$	VCCHx–GND	13.5	15.0	16.5	V
VCCL Pin Voltage	$V_{VCCL}$	VCCL–GND	13.5	15.0	16.5	V
VBx-VSx Pin Voltage	$V_{VBx-VSx}$	VBx–VSx	13.0	15.0	18.5	V
Dead Time of Input Signal	$t_{DEAD}$	INxH, INLx	2.0	—	—	$\mu\text{s}$
PWM Control Frequency	$f_{PWM}$		5	10	20	kHz
INxH Pin Input Pulse Width (On)	$t_{INxH(ON)}$		1.5	—	—	$\mu\text{s}$
INxH Pin Input Pulse Width (Off)	$t_{INxH(OFF)}$		1.5	—	—	$\mu\text{s}$
INxL Pin Input Pulse Width (On)	$t_{INxL(ON)}$		1.5	—	—	$\mu\text{s}$
INxL Pin Input Pulse Width (Off)	$t_{INxL(OFF)}$		1.5	—	—	$\mu\text{s}$
P Pin Capacitor	$C_S$	Ceramic capacitor	0.1	47	—	$\mu\text{F}$
VCCHx/VCCL Pin Capacitor 1	$C_{VCC1}$		22	47	—	$\mu\text{F}$
VCCHx/VCCL Pin Capacitor 2	$C_{VCC2}$	Ceramic capacitor	0.47	1.0	2.2	$\mu\text{F}$
Bootstrap Capacitor 1	$C_{BS1}$		4.7	10	100	$\mu\text{F}$
Bootstrap Capacitor 2	$C_{BS2}$	Ceramic capacitor	0.47	1.0	2.2	$\mu\text{F}$
External VCC Supply Output Current	$I_{VCC}$	$f_{PWM} = 5\text{ kHz}$	21	—	—	mA
		$f_{PWM} = 10\text{ kHz}$	30	—	—	
		$f_{PWM} = 15\text{ kHz}$	39	—	—	
		$f_{PWM} = 20\text{ kHz}$	48	—	—	
VCCxH/VCCL Pin Zener Diode Breakdown Voltage	$V_{Z-DVCC}$	$I_Z = 1\text{ mA}$	16.5	18.2	20.0	V
FO Pin Pull-up Resistor	$R_{FO}$		5.5	10.0	33.0	k $\Omega$
FO Pin Pull-up Voltage	$V_{FO-PU}$		3.0	5.0	5.5	V
FO Pin Capacitor	$C_{FO}$		—	1000	3300	pF
CFO Pin Capacitor	$C_{CFO}$		0.01	0.10	1.00	$\mu\text{F}$
Shunt Resistor*	$R_S$	OCP operating current: 50 A to 100 A	5.4	7.3	9.2	m $\Omega$
OCP RC Filter Time Constant	$t_{RFCF}$	$t_{RFCF} = R_F \times C_F$	0.5	1.0	1.5	$\mu\text{s}$
	$R_F$		—	—	100	$\Omega$
	$C_F$		3300	—	22000	pF
Thermistor Operating Current	$I_{TH}$		—	—	0.2	mA

\* Should be a low-inductance resistor.

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### 4. Electrical Characteristics

Unless specifically noted,  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{VCC_{HX}} = V_{VCC_{L}} = 15\text{ V}$ ,  $R_{FO} = 10\text{ k}\Omega$ ,  $C_{FO} = 0\text{ }\mu\text{F}$ ,  $V_{FO\_PU} = 5\text{ V}$ .

#### 4.1. Characteristics of Control Parts

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
<b>Power Supply Operation</b>							
VCCL Pin Operating Voltage	$V_{VCC_{L\_H}}$		11.2	12.6	13.3	V	Recovering voltage from UVLO
VCCL Pin Operating Stop Voltage	$V_{VCC_{L\_L}}$		10.7	12.1	12.8	V	UVLO detection voltage
VCCL Pin Hysteresis	$V_{VCC_{L\_HYS}}$		—	0.5	—	V	
VBx–VSx Operating Voltage	$V_{VBx\_VSx\_H}$		11.0	12.1	12.8	V	Recovering voltage from UVLO
VBx–VSx Operating Stop Voltage	$V_{VBx\_VSx\_L}$		10.5	11.6	12.3	V	UVLO detection voltage
VBx–VSx Hysteresis	$V_{VBx\_VSx\_HYS}$		—	0.5	—	V	
VCCHx Pin Input Current	$I_{VCCHx}$	$V_{INHx} = 0\text{ V}$ , each pin	—	1.4	2.0	mA	
		$V_{INHx} = 5\text{ V}$ , each pin	—	1.4	2.0		
VCCL Pin Input Current	$I_{VCC_{L}}$	$V_{INLx} = 0\text{ V}$	—	1.9	3.2	mA	
		$V_{INLx} = 5\text{ V}$	—	1.9	3.2		
VBx–VSx Pin Input Current	$I_{VBx\_VSx}$	$V_{VBx\_VSx} = 15\text{ V}$ , $V_{INHx} = 0\text{ V}$ ; 1-phase operation	—	0.09	0.30	mA	
		$V_{VBx\_VSx} = 15\text{ V}$ , $V_{INHx} = 5\text{ V}$ ; 1-phase operation	—	0.11	0.30		
<b>Input Signal</b>							
INHx Pin High-level Input Threshold Voltage	$V_{INHx\_H}$		—	2.0	2.5	V	
INHx Pin Low-level Input Threshold Voltage	$V_{INHx\_L}$		1.0	1.5	—	V	
INHx Pin Hysteresis	$V_{INHx\_HYS}$		—	0.5	—	V	
INLx Pin High-level Input Threshold Voltage	$V_{INLx\_H}$		—	2.0	2.5	V	
INLx Pin Low-level Input Threshold Voltage	$V_{INLx\_L}$		1.0	1.5	—	V	
INLx Pin Hysteresis	$V_{INLx\_HYS}$		—	0.5	—	V	
INHx Pin Input Current	$I_{INHx}$	$V_{INHx} = 5\text{ V}$ , each pin	—	0.25	0.50	mA	
INLx Pin Input Current	$I_{INLx}$	$V_{INLx} = 5\text{ V}$ , each pin	—	0.25	0.50	mA	
<b>Fault Signal Output, Shutdown Signal Input</b>							
FO Pin Shutdown Release Voltage	$V_{FO\_H}$		—	2.0	2.5	V	
FO Pin Shutdown Threshold Voltage	$V_{FO\_L}$		1.0	1.5	—	V	
FO Pin Shutdown Hysteresis	$V_{FO\_HYS}$		—	0.5	—	V	
FO Pin Output Voltage in Normal Operation	$V_{FO(OUT)\_H}$	$V_{FO\_PU} = 5\text{ V}$ , $R_{FO} = 10\text{ k}\Omega$ , $V_{OCP} = 0\text{ V}$	4.8	5.0	—	V	
FO Pin Fault Signal Output Voltage	$V_{FO(OUT)\_L}$	$V_{FO\_PU} = 5\text{ V}$ , $R_{FO} = 10\text{ k}\Omega$ , $V_{OCP} = 1\text{ V}$	—	0.05	0.50	V	

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Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
FO Pin OCP Hold Time <sup>(1)</sup>	t <sub>FO</sub>	C <sub>CF0</sub> = 0 μF	0.012	0.030	0.060	ms	
		C <sub>CF0</sub> = 0.001 μF	0.20	0.32	0.44	ms	
		C <sub>CF0</sub> = 0.01 μF	2.0	3.2	4.4	ms	
		C <sub>CF0</sub> = 0.1 μF	20	32	44	ms	
		C <sub>CF0</sub> = 1 μF	200	320	440	ms	
<b>Protection</b>							
OCP Pin Overcurrent Detection Voltage	V <sub>OCP_H</sub>		0.46	0.50	0.54	V	
OCP Pin Overcurrent Release Voltage	V <sub>OCP_L</sub>		0.32	0.38	0.44	V	
OCP Pin Overcurrent Hysteresis	V <sub>OCP_HYS</sub>		—	0.12	—	V	
OCP Pin Detection Delay Time	t <sub>OCP_DELAY</sub>	<sup>(2)</sup>	—	0.7	1.5	μs	
OCP Pin Filter Time <sup>(3)</sup>	t <sub>OCP_FILTER</sub>		—	0.3	0.5	μs	
OCP Pin Input Current	I <sub>OCP</sub>	V <sub>OCP</sub> = 0.5 V	—	0	—	mA	

<sup>(1)</sup> The shipping test is performed with the condition at C<sub>CF0</sub> = 0.01 μF only.

<sup>(2)</sup> For the measurement circuit for the OCP Pin Detection Delay Time, see Figure 4-1 (all the pins that are not represented in the figure are open). Figure 4-2 provides the definition of the OCP Pin Detection Delay Time.

<sup>(3)</sup> Guaranteed by design.

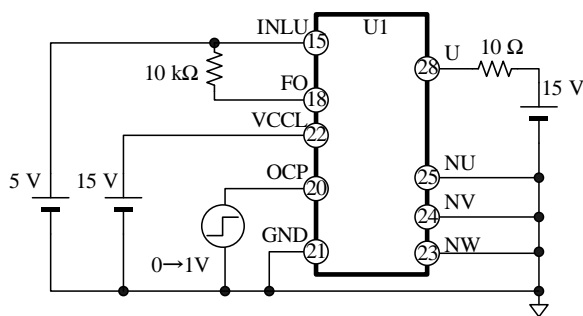


Figure 4-1. Measurement Circuit for OCP Pin Detection Delay Time

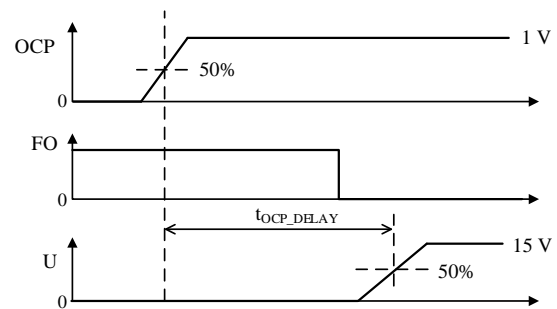


Figure 4-2. OCP Pin Detection Delay Time Definition



**4.2. Bootstrap Diode Characteristics**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Bootstrap Diode Forward Voltage Drop	$V_{F\_BS}$	$I_{F\_BS} = 0.01 \text{ A}$	0.4	0.9	1.4	V	Including voltage drop of series resistor
		$I_{F\_BS} = 0.1 \text{ A}$	2.0	3.0	4.0	V	
Bootstrap Diode Series Resistor*	$R_{S\_BS}$		12	20	28	$\Omega$	

\* Guaranteed by design.

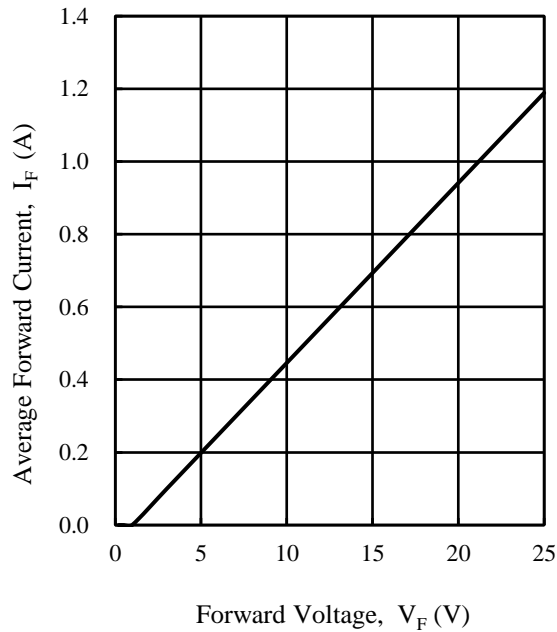


Figure 4-3. Bootstrap Diode Typical Characteristics:  $I_F$  vs.  $V_F$  ( $T_J = 25 \text{ }^\circ\text{C}$ )

**4.3. Thermistor Characteristics**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Thermistor Resistance <sup>(1)(2)</sup>	R <sub>25</sub>	T <sub>A</sub> = 25 °C	—	100.0	—	kΩ	
Thermistor B Constant <sup>(1)</sup>	B <sub>25-85</sub>	T <sub>TH</sub> = 25 °C, 85 °C	—	4395	—	K	

\* Guaranteed by design.

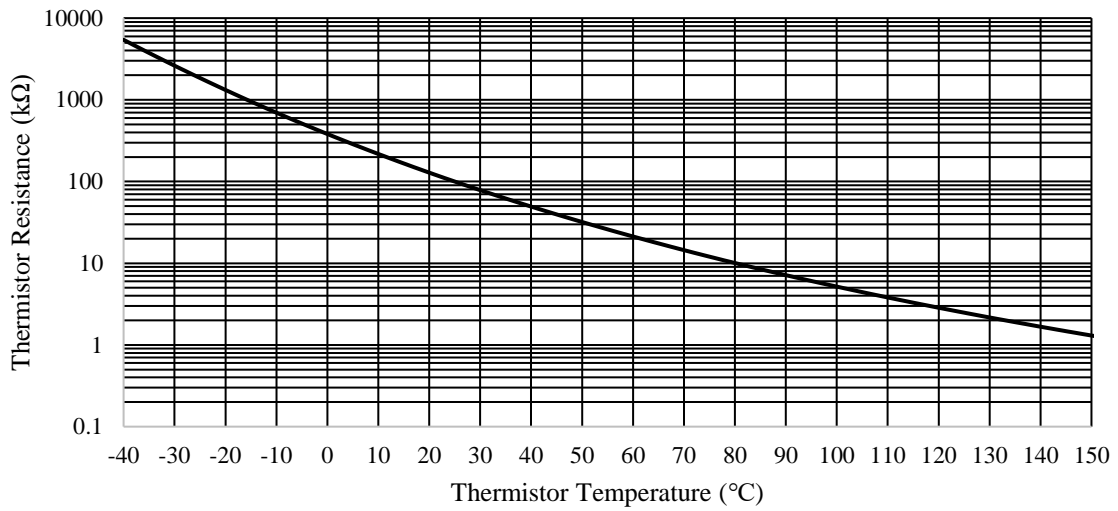


Figure 4-4. Reference Thermistor Resistance

<sup>(1)</sup> Guaranteed by design.

<sup>(2)</sup> For the reference thermistor resistance, see Figure 4-4 and Table 4-1.

Table 4-1. Reference Thermistor Resistance

Thermistor Temperature (°C)	Thermistor Resistance Typ. (kΩ)	Thermistor Temperature (°C)	Thermistor Resistance Typ. (kΩ)
-40	5427	105	4.43
-35	3748	110	3.81
-30	2619	115	3.29
-25	1850	120	2.85
-20	1321	125	2.48
-15	954	130	2.17
-10	696	135	1.90
-5	513	140	1.67
0	382	145	1.47
5	287	150	1.30
10	218		
15	166		
20	128		
25	100		
30	78.4		
35	62.0		
40	49.4		
45	39.6		
50	32.0		
55	26.0		
60	21.3		
65	17.5		
70	14.5		
75	12.0		
80	10.1		
85	8.46		
90	7.15		
95	6.07		
100	5.17		

**4.4. Thermal Resistance Characteristics**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Junction-to-Case Thermal Resistance <sup>(1)(2)</sup>	$R_{(J-C)Q}$ <sup>(3)</sup>	1 element operating (IGBT)	—	—	1.0	°C/W
	$R_{(J-C)F}$ <sup>(4)</sup>	1 element operating (freewheeling diode)	—	—	2.0	°C/W

<sup>(1)</sup> Guaranteed by design.

<sup>(2)</sup> Refers to a case temperature at the measurement point described in Figure 4-5.

<sup>(3)</sup> Refers to steady-state thermal resistance between the junction of the built-in IGBTs and the case.

<sup>(4)</sup> Refers to steady-state thermal resistance between the junction of the built-in freewheeling diodes and the case.

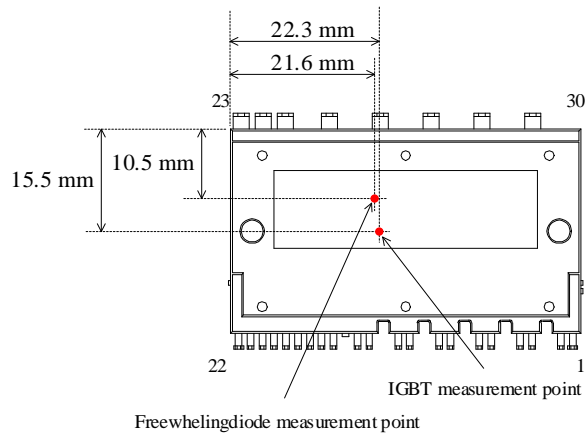


Figure 4-5. Case Temperature Measurement Point

4.5. Transistor Characteristics

Figure 4-6 provides the definitions of switching characteristics described in this and the following sections.

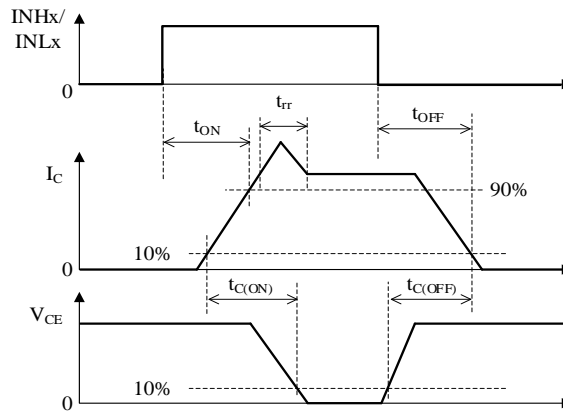


Figure 4-6. Switching Characteristics Definitions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	$I_{CES}$	$V_{CE} = 650 \text{ V}, T_J = 25 \text{ }^\circ\text{C}$	—	—	0.1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 50 \text{ A}, T_J = 25 \text{ }^\circ\text{C}$	—	1.70	2.20	V
		$I_C = 50 \text{ A}, T_J = 125 \text{ }^\circ\text{C}$	—	2.00	2.50	V
Diode Forward Voltage Drop	$V_F$	$I_F = 50 \text{ A}, T_J = 25 \text{ }^\circ\text{C}$	—	2.0	2.5	V
<b>High-side Switching</b>						
Diode Reverse Recovery Time*	$t_{rr}$	$V_{DC} = 300 \text{ V}, I_C = 50 \text{ A}, V_{IN} = 0 \leftrightarrow 5 \text{ V}, T_J = 25 \text{ }^\circ\text{C};$ inductive load	—	0.35	—	$\mu\text{s}$
Turn-on Time*	$t_{ON}$		—	0.65	—	$\mu\text{s}$
Turn-on Switching Time*	$t_{C(ON)}$		—	0.15	—	$\mu\text{s}$
Turn-off Time*	$t_{OFF}$		—	1.45	—	$\mu\text{s}$
Turn-off Switching Time*	$t_{C(OFF)}$		—	0.15	—	$\mu\text{s}$
<b>Low-side Switching</b>						
Diode Reverse Recovery Time*	$t_{rr}$	$V_{DC} = 300 \text{ V}, I_C = 50 \text{ A}, V_{IN} = 0 \leftrightarrow 5 \text{ V}, T_J = 25 \text{ }^\circ\text{C};$ inductive load	—	0.35	—	$\mu\text{s}$
Turn-on Time*	$t_{ON}$		—	0.50	—	$\mu\text{s}$
Turn-on Switching Time*	$t_{C(ON)}$		—	0.20	—	$\mu\text{s}$
Turn-off Time*	$t_{OFF}$		—	0.95	—	$\mu\text{s}$
Turn-off Switching Time*	$t_{C(OFF)}$		—	0.10	—	$\mu\text{s}$

\* Guaranteed by design.

**5. Mechanical Characteristics**

Parameter	Conditions	Min.	Typ.	Max.	Unit
Heatsink Mounting Screw Torque <sup>(1)</sup>	(2)	0.64	0.80	0.96	N·m
		6.6	8.2	9.8	kgf·cm
Flatness of Heatsink Attachment Area <sup>(1)</sup>	See Figure 5-1	0	—	100	μm
Package Weight <sup>(1)</sup>		—	23	—	g

<sup>(1)</sup> Guaranteed by design.

<sup>(2)</sup> Requires using a metric screw of M3 and a plain washer of 7 mm (φ). For more details about screw tightening, see Section 14.2.

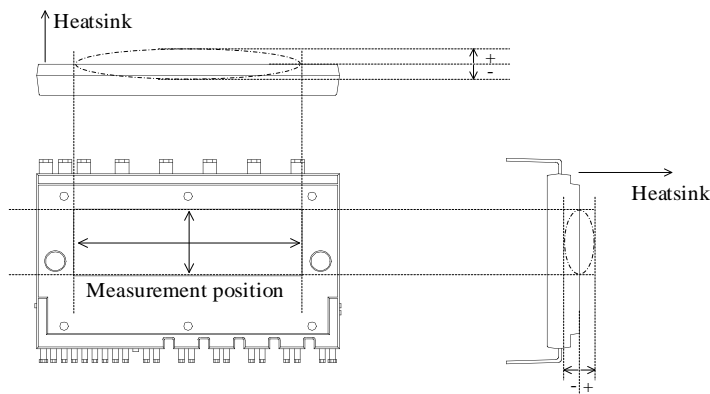


Figure 5-1. Flatness Measurement Position

**6. Insulation Distance**

Parameter	Conditions	Min.	Typ.	Max.	Unit
Clearance <sup>(1)</sup>	Between heatsink and leads. See Figure 6-1.	3.0	3.1	—	mm
Creepage <sup>(1)(2)</sup>		4.2	4.6	—	mm

<sup>(1)</sup> Guaranteed by design.

<sup>(2)</sup> Refers to when a heatsink to be mounted is flat. If your application requires a clearance exceeding the maximum distance given above, use an alternative (e.g., a convex heatsink) that will meet the target requirement.

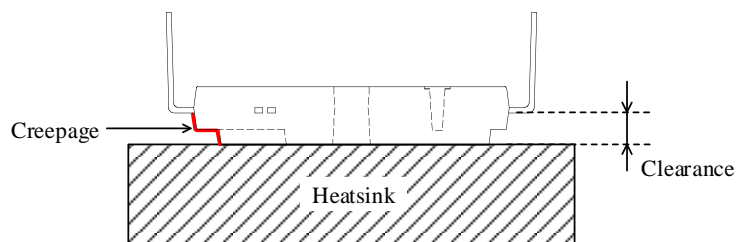


Figure 6-1. Insulation Distance Definitions

**7. Truth Table**

Table 7-1 is a truth table that provides the logic level definitions of operation modes.

In the case where INHx and INLx signals in each phase are high at the same time, both the high- and low-side IGBTs become on (simultaneous on-state). Therefore, the input signals for the INHx and INLx pins, require dead time setting so that such a simultaneous on-state event can be avoided.

Table 7-1. Truth Table for Operation Modes

Mode	INHx	INLx	High-side IGBT	Low-side IGBT	FO Pin Output
Normal Operation	L	L	OFF	OFF	H
	H	L	ON	OFF	
	L	H	OFF	ON	
	H	H	ON	ON	
External Shutdown Signal Input FO = L	L	L	OFF	OFF	—
	H	L	ON	OFF	
	L	H	OFF	OFF	
	H	H	ON	OFF	
VBx Pin Undervoltage Lockout Operation (UVLO_VBx)	L	L	OFF	OFF	H
	H	L	OFF	OFF	
	L	H	OFF	ON	
	H	H	OFF	ON	
VCCL Pin Undervoltage Lockout Operation (UVLO_VCCL)	L	L	OFF	OFF	L
	H	L	ON	OFF	
	L	H	OFF	OFF	
	H	H	ON	OFF	
Overcurrent Protection (OCP)	L	L	OFF	OFF	L
	H	L	ON	OFF	
	L	H	OFF	OFF	
	H	H	ON	OFF	

### 8. Block Diagram

Figure 8-1 shows a block diagram, Figure 8-2 to Figure 8-4 show the internal circuit diagrams of the INHx or INLx pin, the FO pin, and the OCP pin.

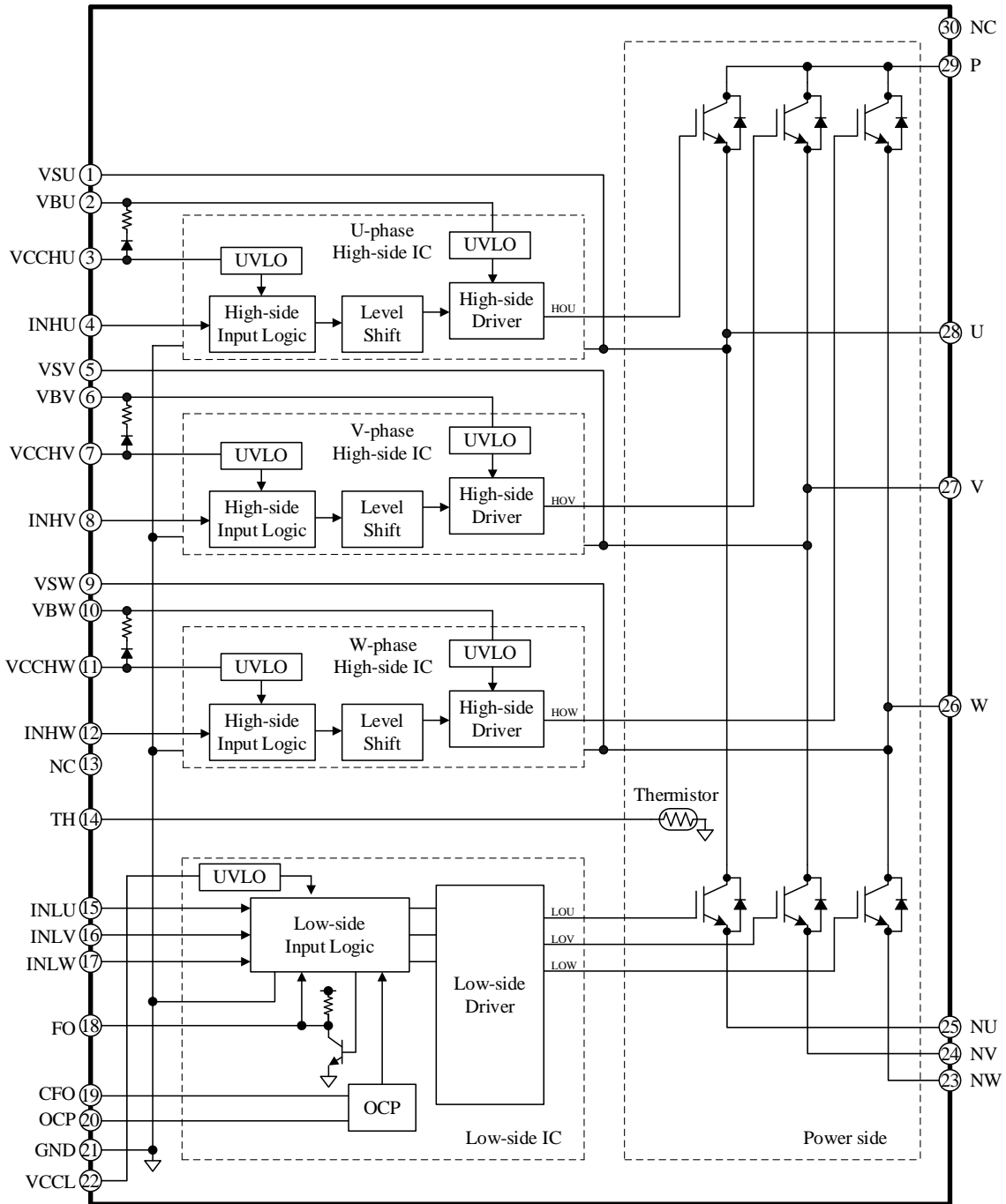


Figure 8-1. Block Diagram



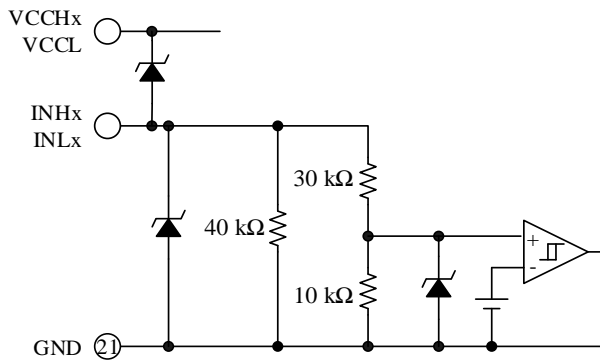


Figure 8-2. Internal Circuit Diagram of INHx, or INLx Pin

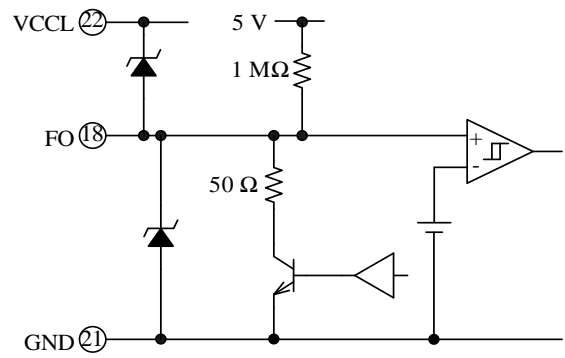


Figure 8-3. Internal Circuit Diagram of FO Pin

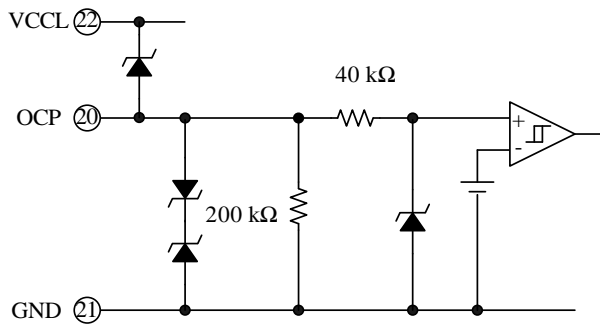
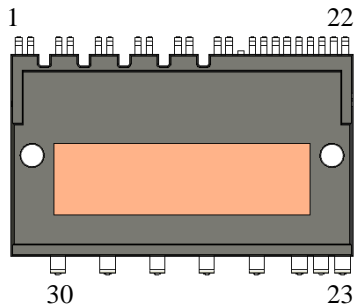


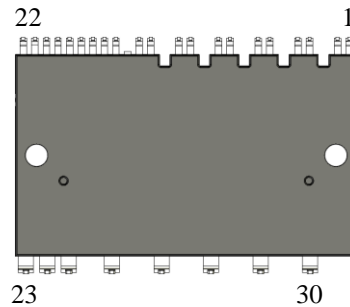
Figure 8-4. Internal Circuit Diagram of OCP Pin

**9. Pin Configuration Definitions**

Top View (Heatsink Side)



Bottom View (Branding Side)



Pin Number	Pin Name	Description
1	VSU	U-phase high-side floating supply ground
2	VBU	U-phase high-side floating supply voltage input
3	VCCHU	U-phase high-side logic supply voltage input
4	INHU	Logic input for U-phase high-side gate driver
5	VSV	V-phase high-side floating supply ground
6	VBV	V-phase high-side floating supply voltage input
7	VCCHV	V-phase high-side logic supply voltage input
8	INHV	Logic input for V-phase high-side gate driver
9	VSW	W-phase high-side floating supply ground
10	VBW	W-phase high-side floating supply voltage input
11	VCCHW	W-phase high-side logic supply voltage input
12	INH W	Logic input for W-phase high-side gate driver
13*	NC	(No connection)
14	TH	Thermistor output
15	INLU	Logic input for U-phase low-side gate driver
16	INLV	Logic input for V-phase low-side gate driver
17	INLW	Logic input for W-phase low-side gate driver
18	FO	Fault signal output and shutdown signal input
19	CFO	Capacitor connection for OCP hold time setting
20	OCP	Input for overcurrent protection
21	GND	Logic ground
22	VCCL	Low-side logic supply voltage input
23	NW	W-phase low-side IGBT emitter
24	NV	V-phase low-side IGBT emitter
25	NU	U-phase low-side IGBT emitter
26	W	W-phase output
27	V	V-phase output
28	U	U-phase output
29	P	Positive DC bus supply voltage
30	NC	(No connection)

\* Pin trimmed.

### 10. Typical Application

CR filters and Zener diodes should be added to your application as needed. This is to protect each pin against surge voltages causing malfunctions, and to avoid the IC being used under the conditions exceeding the absolute maximum ratings where critical damage is inevitable. Then, check all the pins thoroughly under actual operating conditions to ensure that your application works flawlessly.

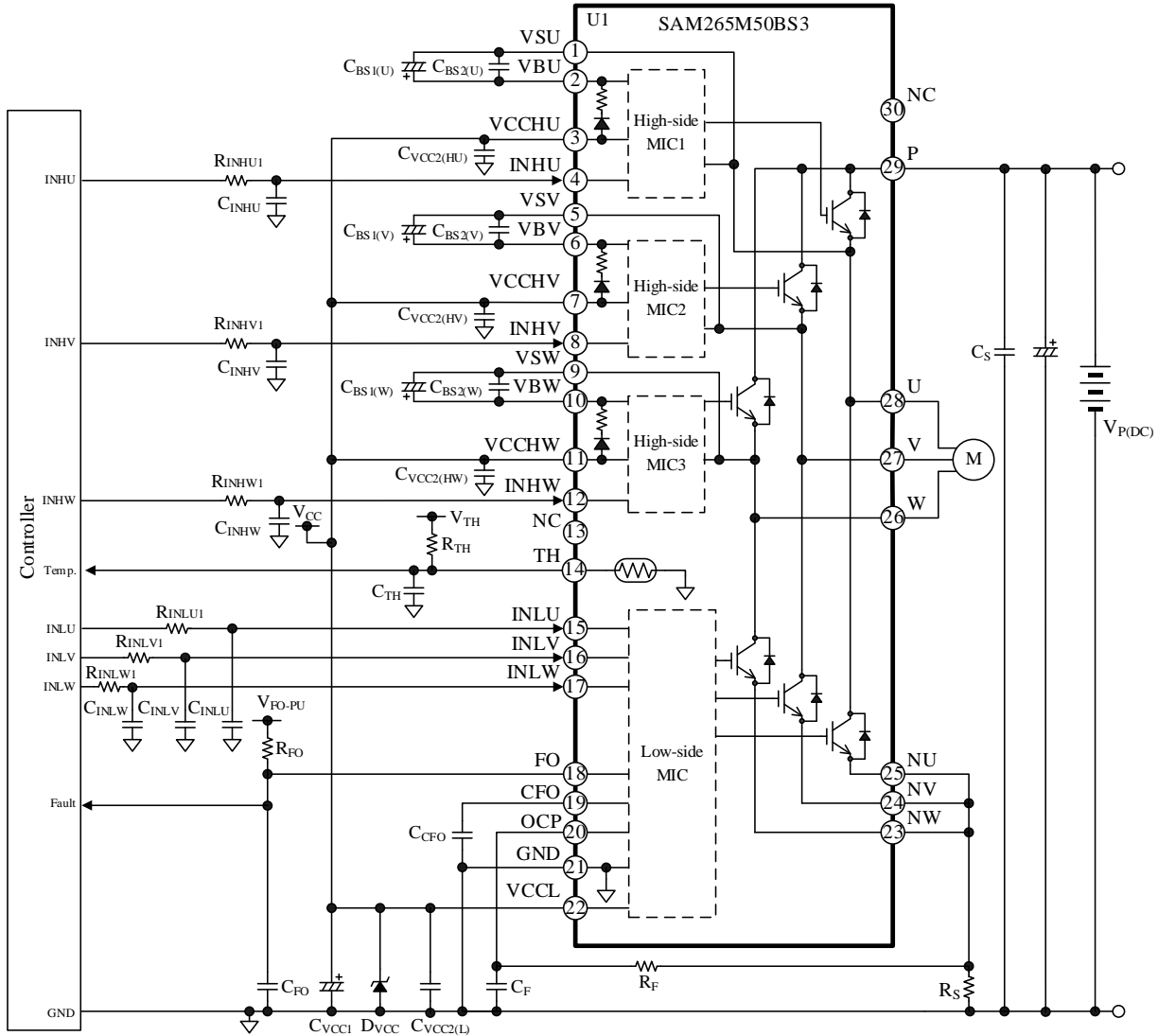


Figure 10-1. Typical Application Using a Single Shunt Resistor

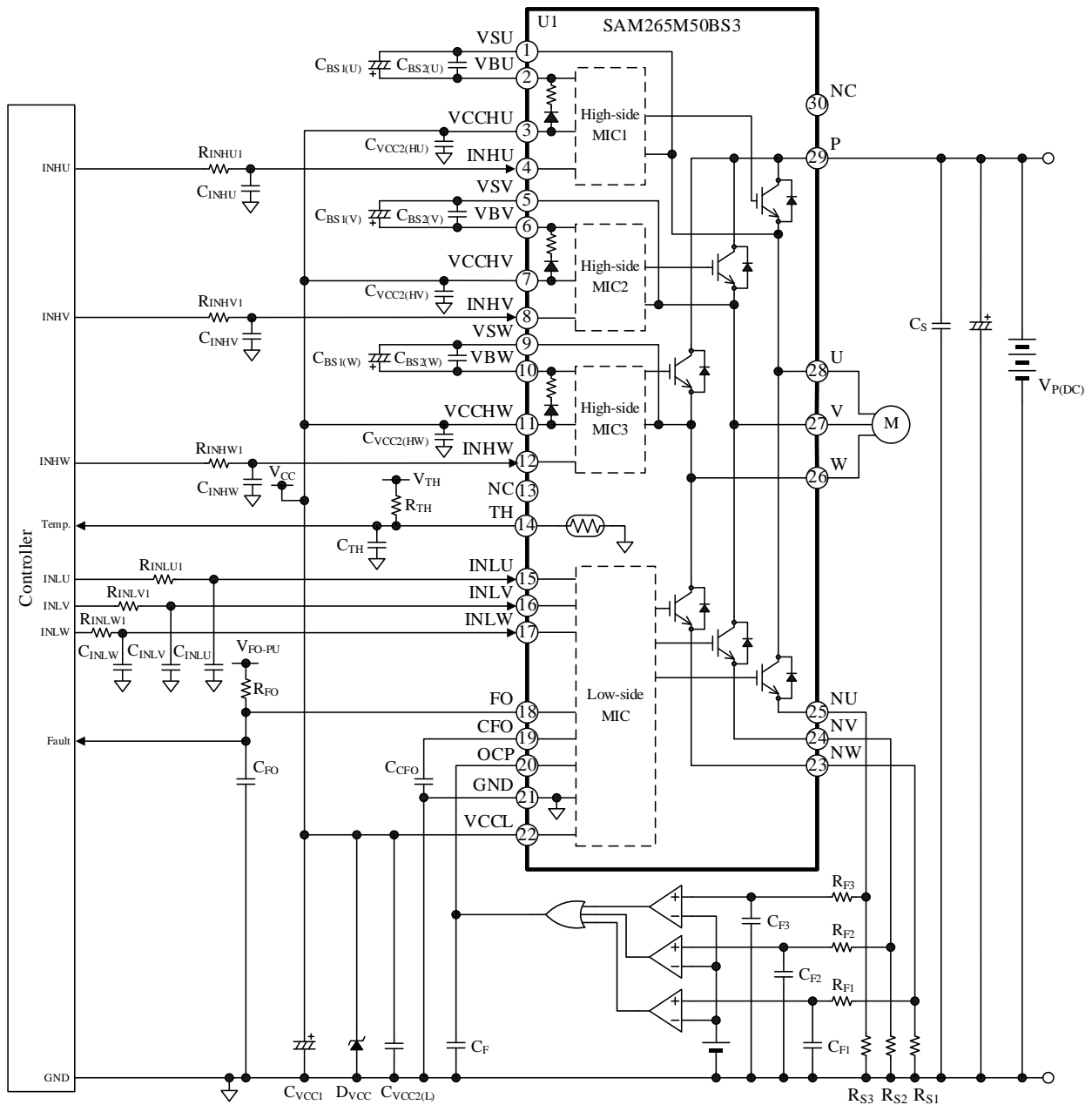
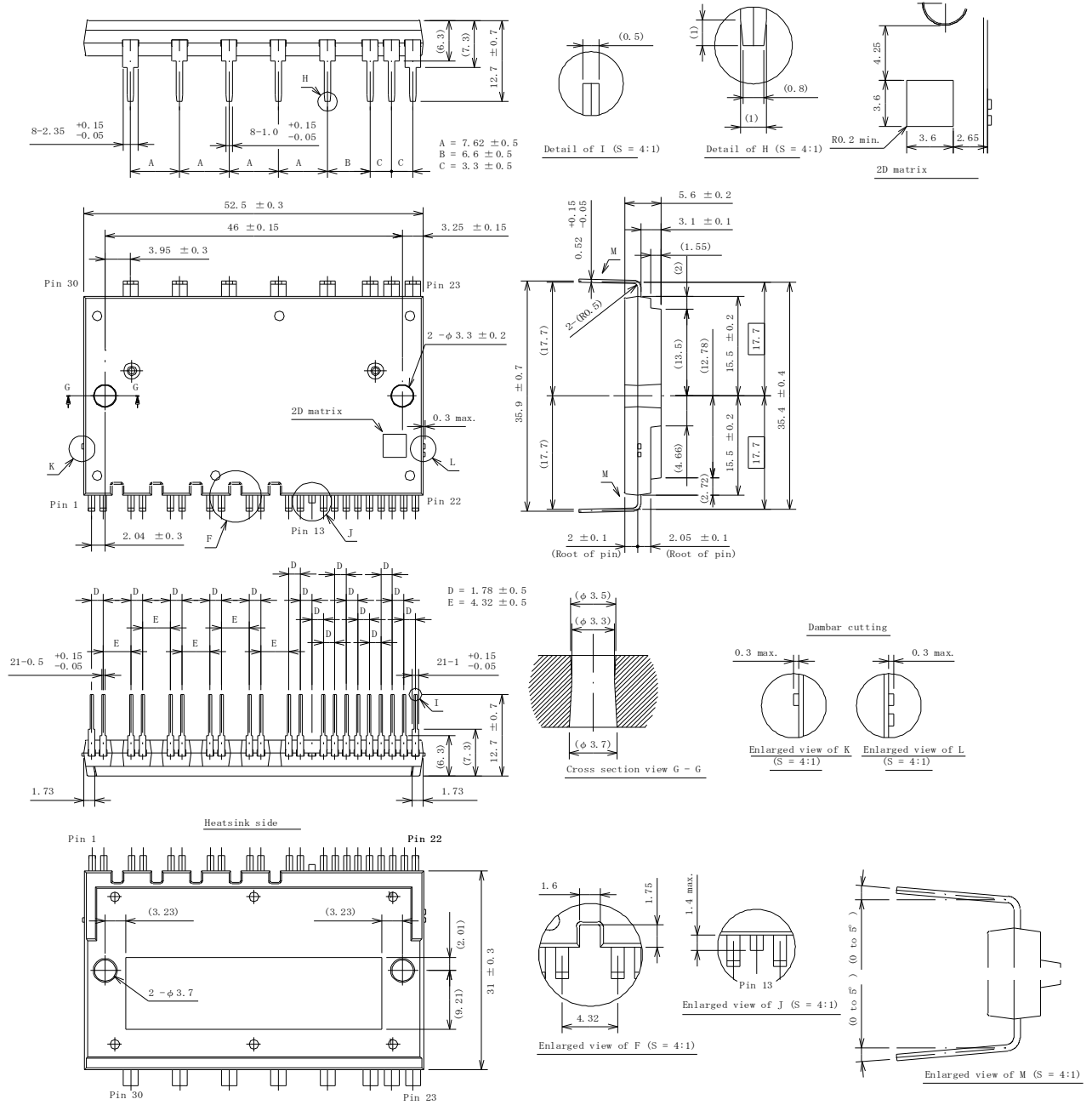


Figure 10-2. Typical Application Using Three Shunt Resistors

**11. Physical Dimensions**

**11.1. DIP30 (Leadform: 2541)**

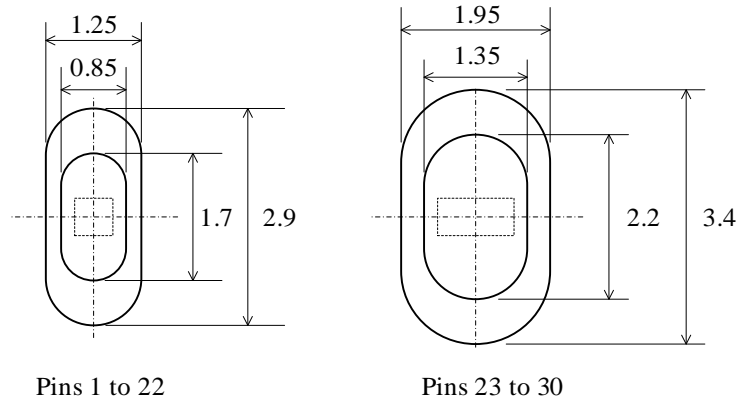


**NOTES:**

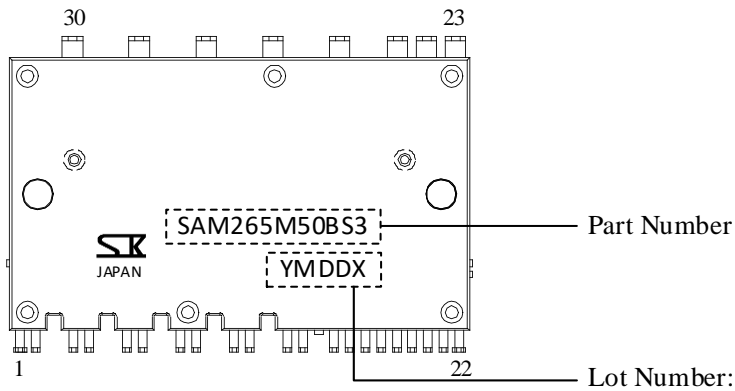
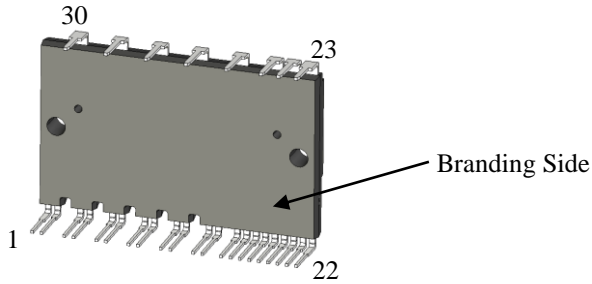
- Dimensions in millimeters
- Pb-free (RoHS compliant)

# SAM265M50BS3

## 11.2. Reference PCB Hole Sizes



## 12. Marking Diagram



Y is the last digit of the year of manufacture (0 to 9)  
M is the month of the year (1 to 9, O, N, or D)  
DD is the day of the month (01 to 31)  
X is the control number

**13. Functional Descriptions**

Unless specifically noted, this section uses the following definitions:

- All the characteristic values given in this section are typical values.
- In the following functional descriptions, “HOx” denotes a gate input signal on the high-side IGBT, whereas “LOx” denotes a gate input signal on the low-side IGBT.
- For pin and peripheral component descriptions, this section employs a notation system that denotes a pin name with the arbitrary letter “x”, depending on context. Thus, “R<sub>Sx</sub>” is used when referring to any or all of the resistors R<sub>S1</sub>, R<sub>S2</sub>, and R<sub>S3</sub>.

**13.1. Turning On and Off the IC**

The procedures listed below provide recommended startup and shutdown sequences. To turn on the IC properly, do not apply any voltage on the INHx and INLx pins until the VCCL pin voltage has reached a stable state ( $V_{VCCL\_H} \geq 13.3$  V).

It is required to fully charge bootstrap capacitors, C<sub>BS1(x)</sub> and C<sub>BS2(x)</sub>, at startup (see Section 13.2.4).

To turn off the IC, set the INHx and INLx pins to logic low (or “L”), and then decrease the VCCL pin voltage.

**13.2. Pin Descriptions**

**13.2.1. P**

This is the input pin for the main supply voltage, i.e., the positive DC bus. All of the IGBT collectors of the high-side are connected to this pin. Voltages between the P and Nx pins should be set within the recommended range of the main supply voltage, V<sub>P(DC)</sub>, given in Section 3.

To suppress surge voltages, put a bypass capacitor of  $\geq 0.1$   $\mu$ F, C<sub>P</sub>, near the P pin with a minimal length of PCB traces to the P pin.

**13.2.2. U, V, and W**

These pins are the outputs of the three phases, and serve as the connection terminals to the 3-phase motor. The U, V, and W pins are internally connected to the VSU, VSV, and VSW pins, respectively.

**13.2.3. NU, NV, and NW**

These are the emitter pins of the low-side IGBTs and are externally connected to shunt resistors, R<sub>Sx</sub>.

When connecting a shunt resistor, place it as near as

possible to the IC with a minimum length of traces to the Nx and GND pins.

**13.2.4. VBU, VBV, and VBW**

These are the inputs of the high-side floating power supplies for the individual phases.

Voltages across the VBx and VSx pins should be maintained within the defined range (i.e., the VBx–VSx Pin Voltage, V<sub>VBx-VSx</sub>) in Section 3.

In each phase, a bootstrap capacitor, C<sub>BS1(x)</sub>, should be connected between the VBx and VSx pins. For proper startup, turn on the low-side transistor first, then fully charge the bootstrap capacitor, C<sub>BS1(x)</sub>. For the capacitance of the bootstrap capacitors, C<sub>BS1(x)</sub>, choose the values that satisfy Equations (1) and (2). Note that capacitance tolerance and DC bias characteristics must be taken into account when you choose appropriate values for C<sub>BS1(x)</sub>.

$$C_{BS1(x)} > (63 \times f_{PWM} + 69) \times t_{L(OFF)} \tag{1}$$

$$4.7 \mu F \leq C_{BS1(x)} \leq 100 \mu F \tag{2}$$

In Equation (1), let C<sub>BS1(x)</sub> be the capacitance ( $\mu$ F) of a bootstrap capacitor, f<sub>PWM</sub> be the PWM control frequency (kHz), and t<sub>L(OFF)</sub> be the maximum off-time of the low-side transistor (i.e., the non-charging time of C<sub>BS1(x)</sub>), measured in seconds.

Even while the high-side transistor is not on, voltage across the bootstrap capacitor keeps decreasing due to power dissipation in the IC. When the VBx pin voltage decreases to V<sub>VBx-VSx\_L</sub> or less, the VBx pin undervoltage lockout (UVLO\_VBx) starts operating (see Section 13.3.3.1). Therefore, actual board checking should be done thoroughly to validate that voltage across the VBx pin maintains over 12.3 V ( $V_{VBx} > V_{VBx-VSx\_L}$ ) during a low-frequency operation such as a startup period.

As Figure 13-1 shows, bootstrap diodes, D<sub>B(x)</sub>, and current-limiting resistors, R<sub>B(x)</sub>, are internally placed in series between the VCCHx and VBx pins. Time constant for the charging time of C<sub>BS1(x)</sub>,  $\tau$ , can be computed by Equation (3):

$$\tau = C_{BS1(x)} \times R_{B(x)} \tag{3}$$

where C<sub>BS1(x)</sub> is the optimized capacitance of the bootstrap capacitor, and R<sub>B(x)</sub> is the resistance of the current-limiting resistor ( $20 \Omega \pm 20\%$ ).

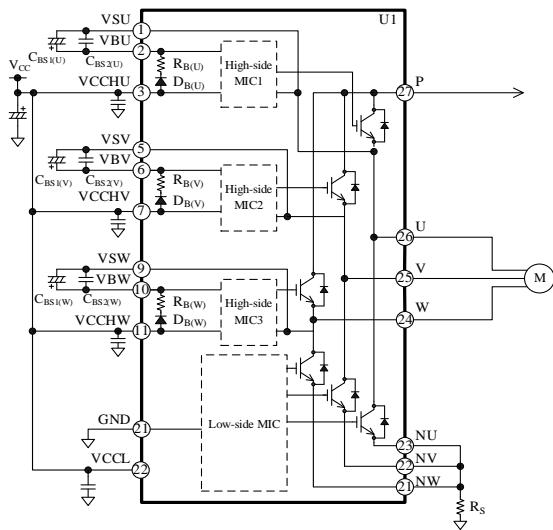


Figure 13-1. Bootstrap Circuit

Figure 13-2 shows an internal level-shifting circuit. And Figure 13-3 shows operational waveforms of the level-shifting circuit. A high-side output signal, HOx, is generated according to an input signal on the INHx pin. When an input signal on the INHx pin transits from low to high (rising edge), a “Set” signal is generated. When the INHx input signal transits from high to low (falling edge), a “Reset” signal is generated. These two signals are then transmitted to the high-side by the level-shifting circuit and are input to the SR flip-flop circuit. Finally, the SR flip-flop circuit feeds an output signal, Q (i.e., HOx).

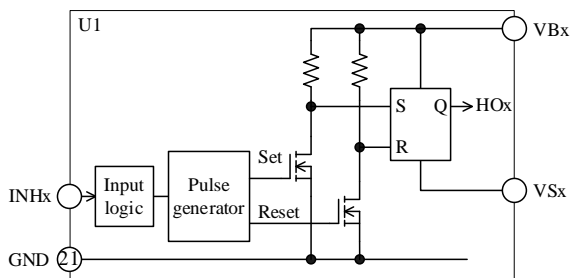


Figure 13-2. Internal Level-shifting Circuit

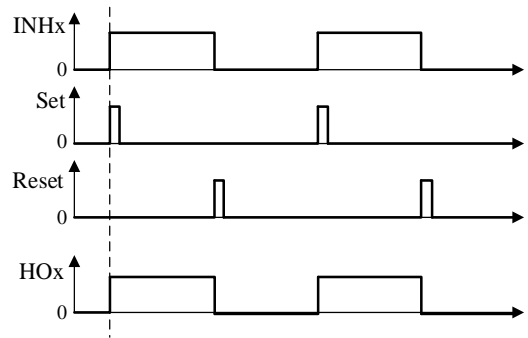


Figure 13-3. Operational Waveforms of Level-shifting Circuit

### 13.2.5. VSU, VSV, and VSW

These pins are the grounds of the high-side floating power supplies for each phase, and are connected to the negative nodes of bootstrap capacitors,  $C_{BS1(X)}$  and  $C_{BS2(X)}$ . The VSU, VSV, and VSW pins are internally connected to the U, V, and W pins, respectively.

### 13.2.6. VCCHU, VCCHV, VCCHW, and VCCL

The VCCHU, VCCHV, and VCCHW pins are the power supply pins for the built-in high-side control MICs. The VCCL pin is the power supply pin for the built-in low-side control MIC. The VCCHx and VCCL pins must be externally connected on a PCB because they are not internally connected. To prevent malfunction induced by supply ripples or other factors, connect a capacitor of  $\geq 22 \mu\text{F}$  ( $C_{VCC1}$ ) and a capacitor of  $0.47 \mu\text{F}$  to  $2.2 \mu\text{F}$  ( $C_{VCC2(L)}$ ) between the VCCL and GND pins with a minimal length of traces. In addition, connect a capacitor of  $0.47 \mu\text{F}$  to  $2.2 \mu\text{F}$  ( $C_{VCC2(Hx)}$ ) between the VCCHx and GND pins with a minimal length of traces.

To prevent damage caused by surge voltages, put a 16.5 V to 20 V Zener diode,  $D_{VCC}$ , between the VCCL and GND pins.

Voltage to be applied between the VCCHx and GND pins should be regulated within the recommended operational range of  $V_{VCCHx}$ , given in Section 3. Voltage to be applied between the VCCL and GND pins should be regulated within the recommended operational range of  $V_{VCCL}$ , given in Section 3.



13.2.7. GND

This is the logic ground pins for the IC. For proper control, the control parts of the IC must be connected to the GND pin. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect the logic ground as close and short as possible to a shunt resistor,  $R_s$ , at a single-point ground (or star ground) which is separated from the power ground (see Figure 13-4). Moreover, extreme care should be taken in designing a PCB so that currents from the power ground do not affect the GND pin.

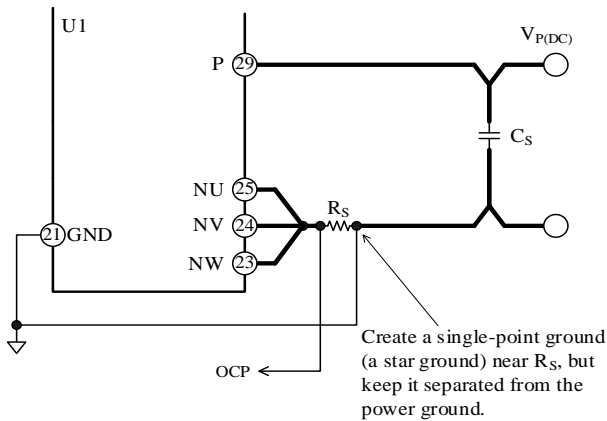


Figure 13-4. Connections to Logic Ground

13.2.8. INHU, INHV, and INHW; INLU, INLV, and INLW

These are the input pins of the internal motor drivers for each phase. The INHx pin acts as a high-side controller; the INLx pin acts as a low-side controller. Figure 13-5 shows an internal circuit diagram of the INHx or INLx pin. This is a comparator circuit with a built-in pull-down resistor.

Input signals across the INHx-GND and the INLx-GND pins in each phase should be set within the ranges provided in Table 13-1, below. Note that dead time setting must be done for INHx and INLx signals because the IC does not have a dead time generator.

The higher PWM carrier frequency rises, the more switching loss increases. Hence, the PWM carrier frequency must be set so that operational case temperatures and junction temperatures have sufficient margins against the absolute maximum ranges, specified in Section 2.

If the signals from the microcontroller become unstable, the IC may result in malfunctions. To avoid such malfunctions, set the microcontroller output line not to have high-impedance outputs. Also, if the traces from the microcontroller to the INHx or INLx pin (or both) are too long, the traces may be interfered by noise. Therefore, it is recommended to add an additional filter

or a pull-down resistor near the INHx or INLx pin as needed (see Figure 13-6).

Here are filter circuit constants for reference:

$R_{INH1x}, R_{INL1x}$ : 47  $\Omega$  to 220  $\Omega$

$R_{INH2x}, R_{INL2x}$ : 1 k $\Omega$  to 10 k $\Omega$

$C_{INHx}, C_{INLx}$ : 100 pF to 1500 pF

Care should be taken in adding  $R_{INH1x}, R_{INL1x}, R_{INH2x}$ , and  $R_{INL2x}$  to the traces. When they are connected to each other, the input voltage of the INHx and INLx pins becomes slightly lower than the output voltage of the microcontroller.

Table 13-1. Input Signals for INHx and INLx Pins

Parameter	High Level Signal	Low Level Signal
Input Voltage	$3\text{ V} < V_{IN} < 5\text{ V}$	$0\text{ V} < V_{IN} < 0.5\text{ V}$
Input Pulse Width	$\geq 1.5\ \mu\text{s}$	$\geq 1.5\ \mu\text{s}$
PWM Carrier Frequency	$5\text{ kHz} \leq f_{sw} \leq 20\text{ kHz}$	
Dead Time	$\geq 2.0\ \mu\text{s}$	

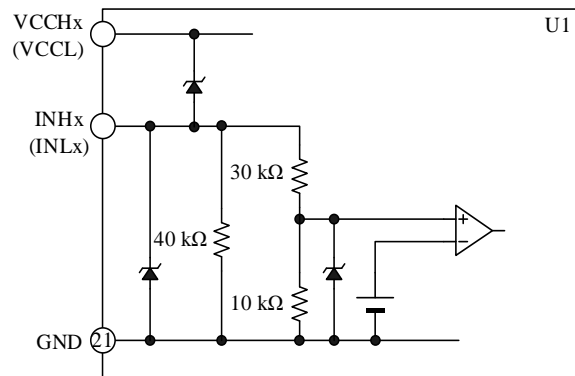


Figure 13-5. Internal Circuit Diagram of INHx or INLx Pin

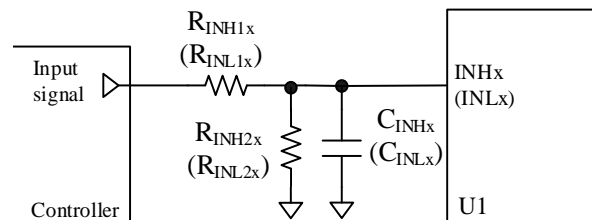


Figure 13-6. Filter Circuit for INHx or INLx Pin

13.2.9. OCP

This pin serves as the input of the overcurrent protection (OCP) which monitors the currents flowing through the low-side output transistors. Section 13.3.4

provides further information about the OCP circuit configuration and its mechanism.

**13.2.10. CFO**

The CFO pin determines the FO Pin OCP Hold Time,  $t_{FO}$ , during the overcurrent protection (OCP) operation. To set  $t_{FO}$ , connect a capacitor,  $C_{CFO}$ , between the CFO and GND pins. Figure 13-7 shows how the OCP hold time,  $t_{FO}$ , and the capacitor,  $C_{CFO}$ , are related.  $C_{CFO}$  should have a capacitance of 0.01  $\mu$ F to 1.00  $\mu$ F.

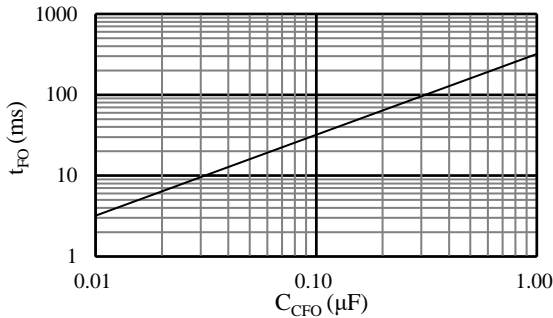


Figure 13-7. CFO Pin Capacitor,  $C_{CFO}$  vs. FO Pin OCP Hold Time,  $t_{FO}$

**13.2.11. FO**

This pin operates as the fault signal output and the shutdown signal input. Sections 13.3.1 and 13.3.2 explain the two functions in detail, respectively.

Figure 13-8 illustrates an internal circuit diagram of the FO pin and its peripheral circuit. Because of its open-collector nature, the FO pin should be tied by a pull-up resistor,  $R_{FO}$ , to the external power supply. The external power supply voltage (i.e., the FO Pin Pull-up Voltage,  $V_{FO\_PU}$ ) should range from 3.0 V to 5.5 V. Therefore, it is recommended to use a 5.5 k $\Omega$  to 33 k $\Omega$  pull-up resistor.

To suppress noise, add a filter capacitor,  $C_{FO}$ , near the IC with minimizing a trace length between the FO and GND pins. The value of  $C_{FO}$  must be set to  $\leq 3300$  pF.

For avoiding repeated OCP activations, the external microcontroller must shut off any input signals to the IC within a fixed hold time,  $t_{FO}$ , after the internal MOSFET ( $Q_{FO}$ ) turn-on.  $t_{FO}$  is the value where minimum values of thermal characteristics are taken into account (for more details, see Section 13.3.4).

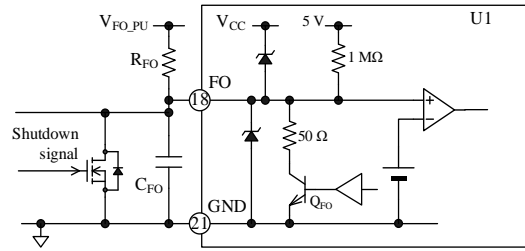


Figure 13-8. Internal Circuit Diagram of FO Pin and Its Peripheral Circuit

**13.2.12. TH**

The SAM265M50BS3 incorporates a thermistor which monitors the temperatures inside the IC.

Figure 13-9 illustrates an internal circuit diagram of the TH pin and its peripheral circuit. The both ends of the internal thermistor are connected to the TH and GND pins, respectively.

Connect a noise filter capacitor,  $C_{TH}$ , between the TH and GND pins.  $C_{TH}$  should have a capacitance of  $\geq 0.1$   $\mu$ F. Then, place  $C_{TH}$  as close as possible to the IC, and connect it between the pin connected to the microcontroller and the TH pin with minimizing respective trace lengths.

In addition, connect the external power supply,  $V_{TH\_PU}$ , and the resistor,  $R_{TH}$ , to the TH pin. The external power supply,  $V_{TH\_PU}$ , should have voltages ranging from 3.0 V to 5.5 V. Table 13-2 provides the recommended values for  $R_{TH}$  according to the external power supply.

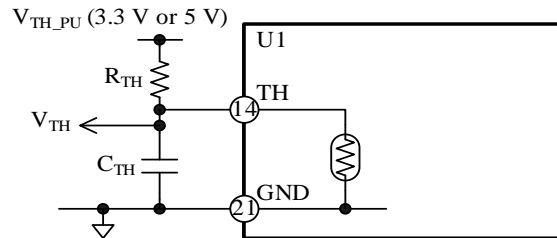


Figure 13-9. Internal Circuit Diagram of TH Pin and Its Peripheral Circuit

Table 13-2. Recommended  $R_{TH}$  Values

$V_{TH\_PU}$ (V)	$R_{TH}$ (k $\Omega$ )		
	Min.	Typ.	Max.
3.3	6.8	15	33
5.0	10	22	47

The following figures show the relationships between the  $V_{TH}$  voltage and the thermistor temperature when  $V_{TH\_PU} = 3.3$  V (Figure 13-10) and when  $V_{TH\_PU} = 5.0$  V

(Figure 13-11). Be sure to set the external power supply,  $V_{TH\_PU}$ , and the resistor,  $R_{TH}$ , according to the thermistor temperature to be detected.

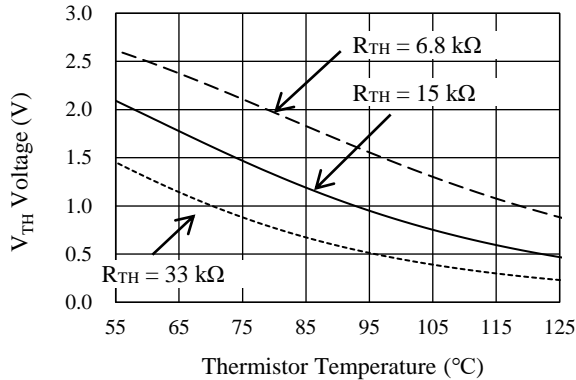


Figure 13-10.  $V_{TH}$  Voltage vs. Thermistor Temperature ( $V_{TH\_PU} = 3.3$  V)

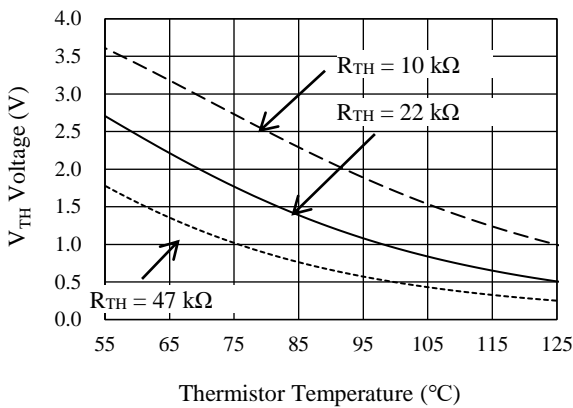


Figure 13-11.  $V_{TH}$  Voltage vs. Thermistor Temperature ( $V_{TH\_PU} = 5.0$  V)

The SAM265M50BS3 does not have any protection against overtemperature; therefore, the motor must be externally controlled when a temperature rise occurs, or be controlled with such protective measures. Moreover, note that the TH pin output does not provide the temperature followability, especially when a rapid temperature rise in the output transistors occurs during motor lock and short circuit conditions.

**13.3. Protection Functions**

This section describes the various protection circuits provided in the SAM265M50BS3. The protection circuits include the VBx pin undervoltage lockout for power supply (UVLO\_VBx), the VCCL pin undervoltage lockout for power supply (UVLO\_VCCL), and the overcurrent protection (OCP).

In case the UVLO\_VCCL or OCP circuit is activated,

the FO pin outputs a fault signal; as a result, the external microcontroller can stop the operations of the three phases by receiving the fault signal. The external microcontroller can also shut down IC operations by inputting a fault signal to the FO pin.

**13.3.1. Fault Signal Output**

In case one or more of the following protections are actuated, an internal transistor,  $Q_{FO}$ , turns on, then the FO pin becomes logic low (0.09 V).

- 1) VCCL pin undervoltage lockout for power supply (UVLO\_VCCL)
- 2) Overcurrent protection (OCP)

While the FO pin is in the low state, all the low-side transistors turn off. In normal operation, the FO pin outputs a high signal of about 5 V. The FO Pin OCP Hold Time,  $t_{FO}$ , is determined by a value of the capacitor,  $C_{CFO}$ , connected to the CFO pin (see Section 13.2.10).

For avoiding repeated OCP activations, the external microcontroller must shut off any input signals to the IC within a fixed hold time,  $t_{FO}$ , after the internal MOSFET ( $Q_{FO}$ ) turn-on.  $t_{FO}$  is the value where minimum values of thermal characteristics are taken into account (for more details, see Section 13.3.4).

**13.3.2. Shutdown Signal Input**

The FO pin also acts as the input pin of shutdown signals. When the FO pin becomes logic low, all the low-side transistors turn off. The voltages and pulse widths of shutdown signals should be set as listed in Table 13-3.

Table 13-3. Shutdown Signals

Parameter	High Level Signal	Low Level Signal
FO Pin Voltage	$3\text{ V} < V_{FO} < 5.5\text{ V}$	$0\text{ V} < V_{FO} < 0.5\text{ V}$
Input Pulse Width	$\geq 3.0\ \mu\text{s}$	$\geq 3.0\ \mu\text{s}$

When the FO pin becomes logic high, all the low-side transistors operate according to input signals to the INLx pin. The FO pin has an internal filter circuit of 2.5  $\mu\text{s}$  to prevent noise-induced malfunctions.

Figure 13-12 shows the operational waveforms at shutdown signal input. Figure 13-13 illustrates an internal circuit diagram of the FO pin and its peripheral circuit.

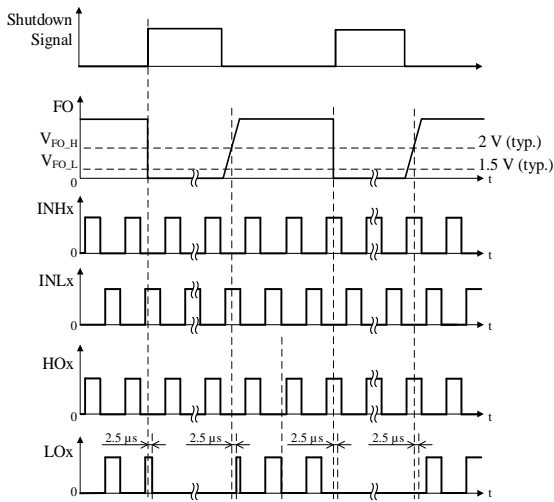


Figure 13-12. Operational Waveforms at Shutdown Signal Input

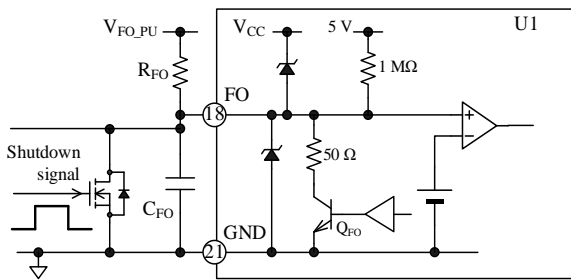


Figure 13-13. Internal Circuit Diagram of FO Pin and Its Peripheral Circuit

### 13.3.3. Undervoltage Lockout for Power Supply (UVLO)

In case the gate-driving voltages of the output transistors decrease, their steady-state power dissipations increase. This overheating condition may cause permanent damage to the IC in the worst case. To prevent this event, the IC has the undervoltage lockout (UVLO) circuits for each of the VBx and VCCL pins.

#### 13.3.3.1. VBx Pin Undervoltage Lockout (UVLO\_VBx)

Figure 13-14 shows operational waveforms of the VBx pin undervoltage lockout for power supply (i.e., UVLO\_VBx).

When the voltage between the VBx and VSx pins (VBx-VSx) decreases to  $V_{VBx-VSx,L} = 11.6$  V or less, the UVLO\_VBx circuit in the corresponding phase gets activated and sets an HOx signal to logic low.

When the voltage between the VBx and VSx pins increases to  $V_{VBx-VSx,H} = 12.1$  V or more, the IC releases

the UVLO\_VBx condition. Then, the HOx signal becomes logic high at the rising edge of the first input command after the UVLO\_VBx release.

Any fault signals are not output from the FO pin during the UVLO\_VBx operation. The VBx pin has an internal filter circuit of about 1.8 μs to prevent noise-induced malfunctions.

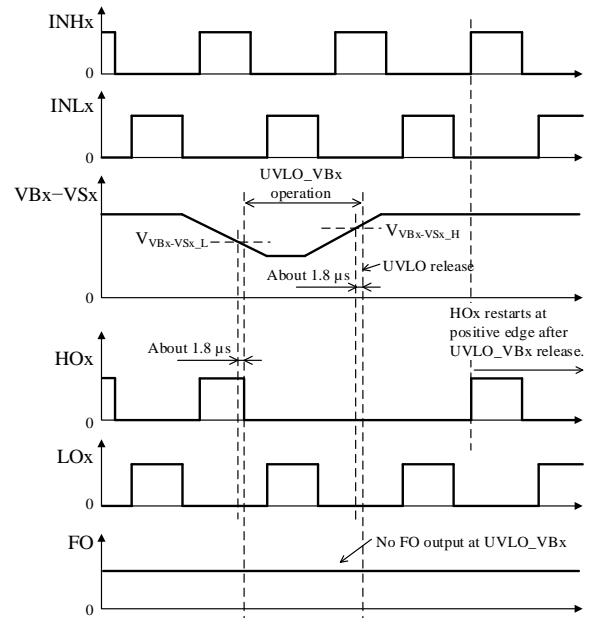


Figure 13-14. UVLO\_VBx Operational Waveforms

#### 13.3.3.2. VCCL Pin Undervoltage Lockout (UVLO\_VCCL)

Figure 13-15 shows operational waveforms of the VCCL pin undervoltage lockout for power supply (i.e., UVLO\_VCCL).

When the VCCL pin voltage decreases to  $V_{VCCL,L} = 12.1$  V or less, the UVLO\_VCCL circuit gets activated and sets an LOx signal to logic low.

When the VCCL pin voltage increases to  $V_{VCCL,H} = 12.6$  V or more, the IC releases the UVLO\_VCCL condition. Then it resumes transmitting the LOx signal according to an input command on the INLx pin.

During the UVLO\_VCCL operation, the FO pin becomes logic low and sends fault signals. The VCCL pin has an internal filter circuit of about 1.8 μs to prevent noise-induced malfunctions.

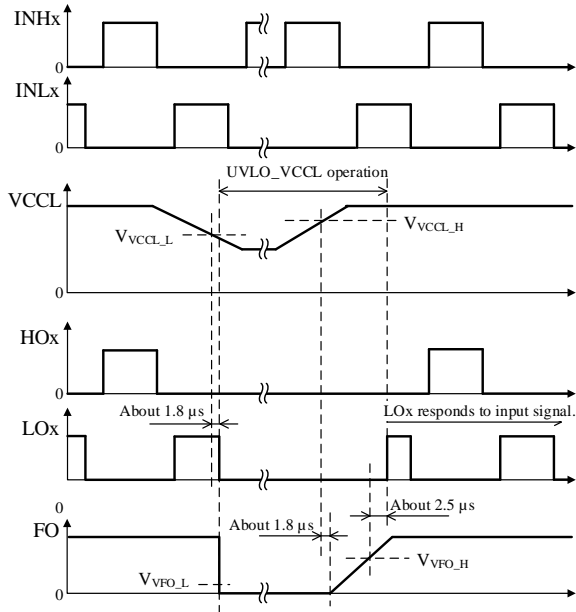


Figure 13-15. UVLO\_VCCCL Operational Waveforms

**13.3.4. Overcurrent Protection (OCP)**

The OCP pin has the overcurrent protection (OCP) circuit. Figure 13-16 is an internal circuit diagram describing the OCP pin and its peripheral circuit.

The OCP pin detects overcurrents with voltage across an external shunt resistor,  $R_S$ . Because the OCP pin is internally pulled down, the OCP pin voltage increases proportionally to a rise in the current running through the shunt resistor,  $R_S$ .

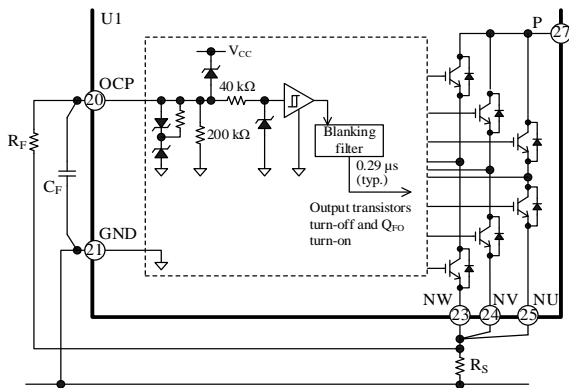


Figure 13-16. Internal Circuit Diagram of OCP Pin and Its Peripheral Circuit

Figure 13-17 shows operational waveforms when the OCP pin detects an overcurrent condition. When the OCP pin voltage increases to  $V_{OCP\_H} = 0.50$  V or more, and remains in this condition for  $0.29 \mu s$  or longer, the OCP circuit is activated. When the OCP is activated, the IC puts an LOx signal and the FO pin to logic low. The

low-side transistors turn off as the LOx signal becomes logic low; as a result, output current decreases. Even if the OCP pin voltage falls below  $V_{OCP\_L}$ , the IC holds the FO pin in the low state for a fixed OCP hold time ( $t_{FO}$ ). The low-side transistors also remain turned off during this period. Then, the output transistors operate according to input signals.

The OCP pin has an internal filter circuit of about  $0.29 \mu s$  to prevent noise-induced malfunctions.

The FO Pin OCP Hold Time,  $t_{FO}$ , is determined by a value of the capacitor,  $C_{CFO}$ , connected to the CFO pin (see Section 13.2.10).

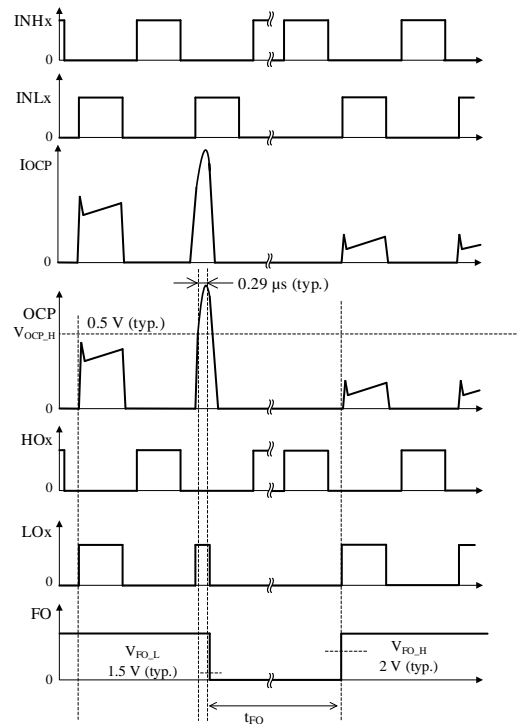


Figure 13-17. OCP Operational Waveforms

The OCP is used for detecting abnormal conditions, such as an output transistor shorted. In case short-circuit conditions occur repeatedly, the output transistors can be destroyed. For this reason, motor operations must be controlled by the external microcontroller so that it can immediately stop the motor when fault signals are detected.

The external microcontroller receives the fault signals with its interrupt pin (INT), and must be programmed to put the INHx and INLx pins to logic low within a predetermined OCP hold time,  $t_{FO}$ . To resume the motor operation thereafter, set the motor to be resumed after a lapse of  $\geq 2$  seconds.

For proper shunt resistor setting, your application must meet the following:

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- Use the shunt resistor that has a recommended resistance,  $R_S$  (see Section 3).
- Set the OCP pin input voltage to vary within the rated OCP pin voltages,  $V_{OCP}$  (see Section 2).
- Keep the current through the output transistors below the rated collector current (peak),  $I_{CP}$  (see Section 2).
- Surface-mount current detection resistor
- Allowable tolerance:  $\pm 2\%$  or less
- Thermal coefficient:  $\pm 200$  ppm/ $^{\circ}\text{C}$  or less

It is required to use a resistor with low internal inductance because high-frequency switching current will flow through the shunt resistor,  $R_S$ . In addition, choose a resistor with allowable power dissipation according to your application.

When you connect a CR filter (i.e., a pair of a filter resistor,  $R_F$ , and a filter capacitor,  $C_F$ ) to the OCP pin, care should be taken in setting the time constants of  $R_F$  and  $C_F$ . The larger the time constant, the longer the time that the OCP pin voltage rises to  $V_{OCP\_H}$ . And this may cause permanent damage to the transistors. Be sure to set the time constants of  $R_F$  and  $C_F$  to  $1.5 \mu\text{s}$  or less so that the OCP can start to operate within  $2.0 \mu\text{s}$  when a short circuit condition occurs. And place  $C_F$  as close as possible to the IC with minimizing a trace length between the OCP and GND pins.

Note that overcurrents are undetectable when one or more of the U, V, and W pins or their traces are shorted to ground (ground fault). In case any of these pins falls into a state of ground fault, the output transistors may be destroyed.



## 14. Design Notes

### 14.1. PCB Pattern Layout

Figure 14-1 shows a schematic diagram of a motor driver circuit. The motor driver circuit consists of current paths having high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing. Current loops (especially, between the P pin,  $C_P$ , and the  $N_x$  pin) should be as small and wide as possible, in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

A shunt resistor,  $R_S$ , should be placed as close as possible to the IC with minimizing a trace length between the  $N_x$  pin and a capacitor,  $C_P$ .

Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect the logic ground as close and short as possible to the shunt resistor,  $R_S$ , at a single-point ground (or star ground) which is separated from the power ground (see Figure 14-1). Moreover, extreme care should be taken when wiring so that currents from the power ground do not affect the logic ground (e.g., the control ground trace is not placed parallel near the power ground, and these traces are not crossed as much as possible).

To reduce the noise effect to the OCP pin, connect the overcurrent detection trace as near as possible to the shunt resistor,  $R_S$  (see Figure 14-1 and Figure 14-2). Also, place the overcurrent detection trace parallel to the logic ground trace and connect it to the OCP pin.

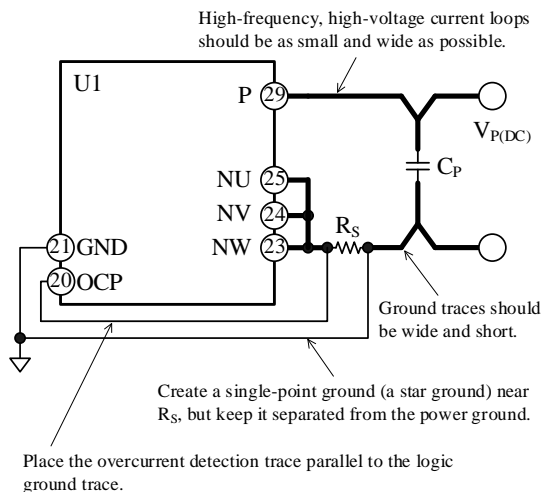


Figure 14-1. High-frequency and High-voltage Current Paths, and Connections to Logic Ground

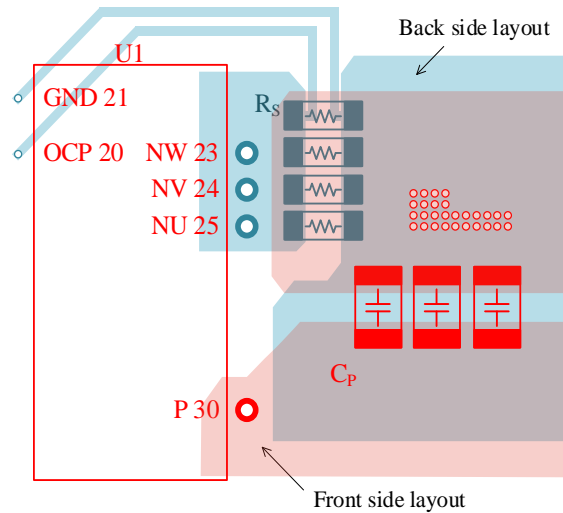


Figure 14-2. Peripheral Layout Example of  $C_P$  (Double-sided Board)

### 14.2. Considerations in Heatsink Mounting

The following are the key considerations and the guidelines for mounting a heatsink:

- Be sure to use a metric screw of M3 and a plain washer of 7 mm ( $\phi$ ). To tighten the screws, use a torque screwdriver. Tighten the two screws firstly up to 20% to 30% of the maximum screw torque, then finally up to 100% of the prescribed maximum screw torque. Perform appropriate tightening within the range of screw torque defined in Section 5. The order of the screws does not matter to the temporary tightening. Note that the sequence when the screws are tightened finally must be the same order as these are tightened firstly.
- When mounting a heatsink, it is recommended to use silicone greases. If a thermally conductive sheet or an electrically insulating sheet is used, package cracks may be occurred due to creases at screw tightening. Therefore, you should conduct thorough evaluations before using these materials.
- When applying a silicone grease, make sure that there are no foreign substances between the IC and a heatsink. Extreme care should be taken not to apply a silicone grease onto any device pins as much as possible. The following requirements must be met for proper grease application:
  - Grease thickness: 100  $\mu\text{m}$  to 200  $\mu\text{m}$

### 14.3. Considerations in IC Characteristics Measurement

When checking the characteristics of the internal switching elements (IGBTs and freewheeling diodes), the IGBTs may result in permanent damage unless these are measured appropriately. Therefore, the following should be taken into account. The absolute maximum rating of the Collector-to-Emitter Voltage,  $V_{CES}$ , is 650 V.

- Do not measure the withstand voltage of the internal IGBTs. Applying the voltage of  $V_{CES}$  or more between the collector and emitter may degrade the IGBTs.
- Measurement condition of the leakage current of the internal IGBTs must be below  $V_{CES}$ .
- The leakage current value is the total leakage current of such as IGBT, freewheeling diode, control IC, and bootstrap diode. These leakage currents can not be measured individually.
- When measuring leakage current of the IGBTs, note that the gate and emitter of the IGBT must be the same potential. To measure the leakage current of the IGBTs, connect each pin as follows:

Measuring the High-side IGBTs:

- Connect the VBx pin to the VSx pin of the corresponding phase.
- Connect the INLx and VCCL pins to the GND pin.
- Connect the VCCHx pin of the to-be-measured phase and the VCCL pin to the GND pin.

Measuring the Low-side IGBTs:

- Connect the VBx pin to the VSx pin of the corresponding phase.
- Connect the INLx and VCCL pins to the GND pin.

The following are circuit diagrams representing typical measurement circuits for leakage current: Figure 14-3 shows the high-side IGBT ( $Q_{LH}$ ) in the U-phase; Figure 14-4 shows the low-side IGBT ( $Q_{LU}$ ) in the U-phase.

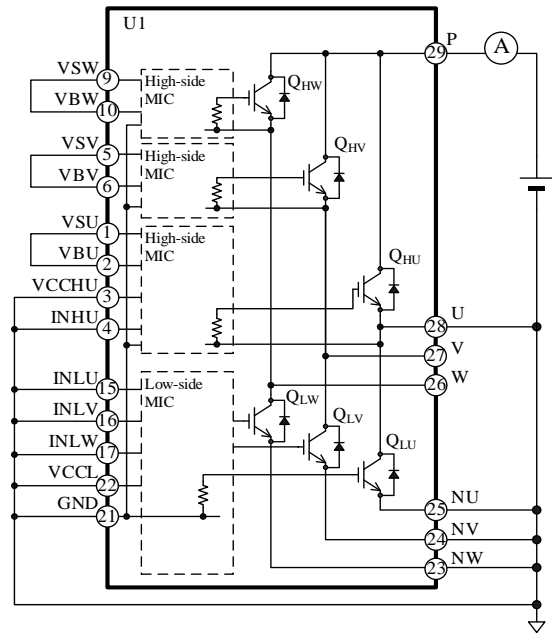


Figure 14-3. Typical Leakage Current Measurement Circuit for High-side IGBT ( $Q_{HU}$ ) in U-phase

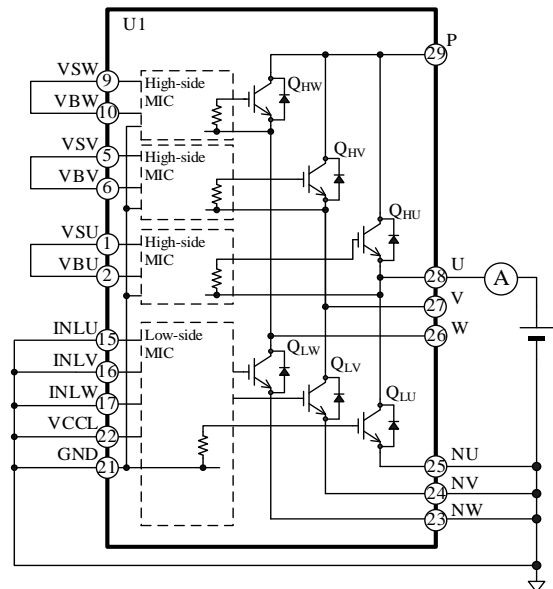


Figure 14-4. Typical Leakage Current Measurement Circuit for Low-side IGBT ( $Q_{LU}$ ) in U-phase



**15. Calculating Power Losses and Estimating Junction Temperature**

This section describes the procedures to calculate power losses in a switching transistor, and to estimate a junction temperature. Note that the descriptions listed here are applicable to the SAM265M50BS3, which is controlled by a 3-phase sine-wave PWM driving strategy.

Total power loss in an IGBT can be obtained by taking the sum of steady-state loss,  $P_{ON}$ , and switching loss,  $P_{SW}$ . The following subsections contain the mathematical procedures to calculate the power losses in an IGBT and its junction temperature.

For quick and easy references, we offer calculation support tools online. Please visit our website to find out more.

- DT0051: SAM265M50BS3 Calculation Tool [https://www.semicon.sanken-ele.co.jp/en/calc-tool/igbt1\\_caltool\\_en.html](https://www.semicon.sanken-ele.co.jp/en/calc-tool/igbt1_caltool_en.html)

**15.1. IGBT Steady-state Loss,  $P_{ON}$**

Figure 15-1 shows the linear approximation ( $V_{CE(SAT)} = \alpha \times I_C + \beta$ ) based on the  $V_{CE(SAT)}$  vs.  $I_C$  curve at a range the  $I_C$  is actually used.

The values gained by the above calculation are then applied as parameters in Equation (4), below. Hence, the equation to obtain the IGBT steady-state loss,  $P_{ON}$ , is:

$$\begin{aligned}
 P_{ON} &= \frac{1}{2\pi} \int_0^\pi V_{CE(SAT)}(\varphi) \times I_C(\varphi) \times DT \times d\varphi \\
 &= \frac{1}{2} \alpha \left( \frac{1}{2} + \frac{4}{3\pi} M \times \cos\theta \right) I_M^2 \\
 &\quad + \frac{\sqrt{2}}{\pi} \beta \left( \frac{1}{2} + \frac{\pi}{8} M \times \cos\theta \right) I_M. \tag{4}
 \end{aligned}$$

Where:

- $V_{CE(SAT)}$  is the collector-to-emitter saturation voltage of the IGBT (V),
- $I_C$  is the collector current of the IGBT (A),
- DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

- M is the modulation index (0 to 1),
- $\cos\theta$  is the motor power factor (0 to 1),
- $I_M$  is the effective motor current (A),
- $\alpha$  is the slope of the linear approximation in the  $V_{CE(SAT)}$  vs.  $I_C$  curve, and
- $\beta$  is the intercept of the linear approximation in the  $V_{CE(SAT)}$  vs.  $I_C$  curve.

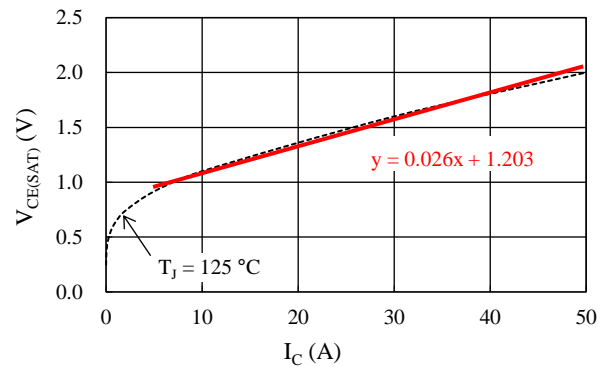


Figure 15-1. Linear Approximate Equation of  $V_{CE(SAT)}$  vs.  $I_C$

**15.2. IGBT Switching Loss,  $P_{SW}$**

Switching loss in an IGBT,  $P_{SW}$ , can be calculated by Equation (5), letting  $I_M$  be the effective current value of the motor:

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{P(DC)}}{300}. \tag{5}$$

Where:

- $f_C$  is the PWM carrier frequency (Hz),
- $V_{P(DC)}$  is the main power supply voltage (V), i.e., the P pin input voltage, and
- $\alpha_E$  is the slope of the switching loss curve (see Section 16.2.2).

**15.3. Estimating Junction Temperature of IGBT**

The junction temperature of an IGBT,  $T_J$ , can be estimated with Equation (6):

$$T_J = R_{(J-C)Q} \times (P_{ON} + P_{SW}) + T_C. \tag{6}$$

Where:

- $R_{(J-C)Q}$  is the junction-to-case thermal resistance per IGBT ( $^{\circ}C/W$ ), and
- $T_C$  is the case temperature ( $^{\circ}C$ ), measured at the point defined in Section 4.4.

## 16. Performance Curves

### 16.1. Transient Thermal Resistance Curves

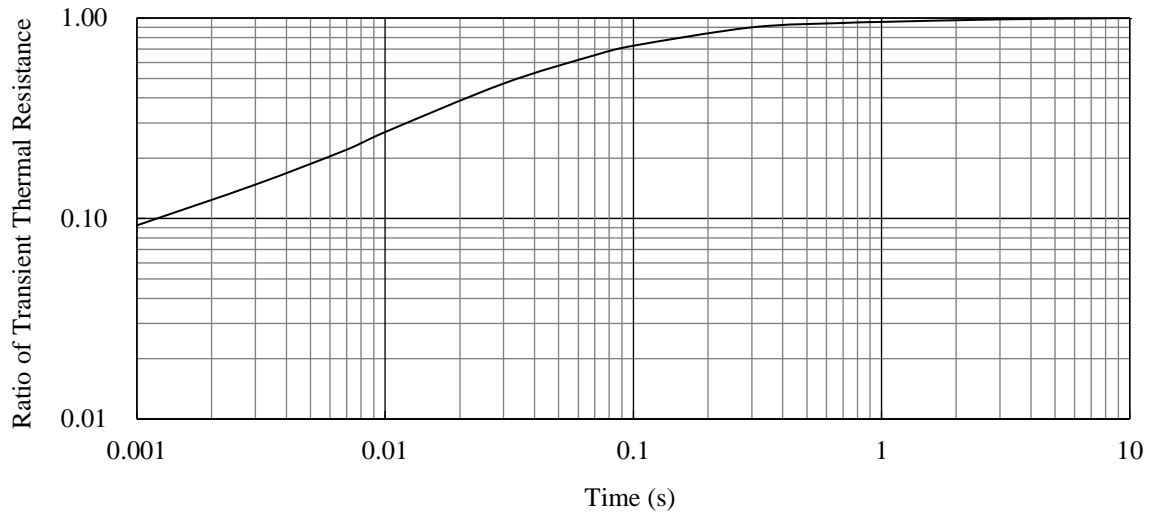


Figure 16-1. Transient Thermal Resistance

16.2. Performance Curves of Output Parts

16.2.1. Output Transistor Performance Curves

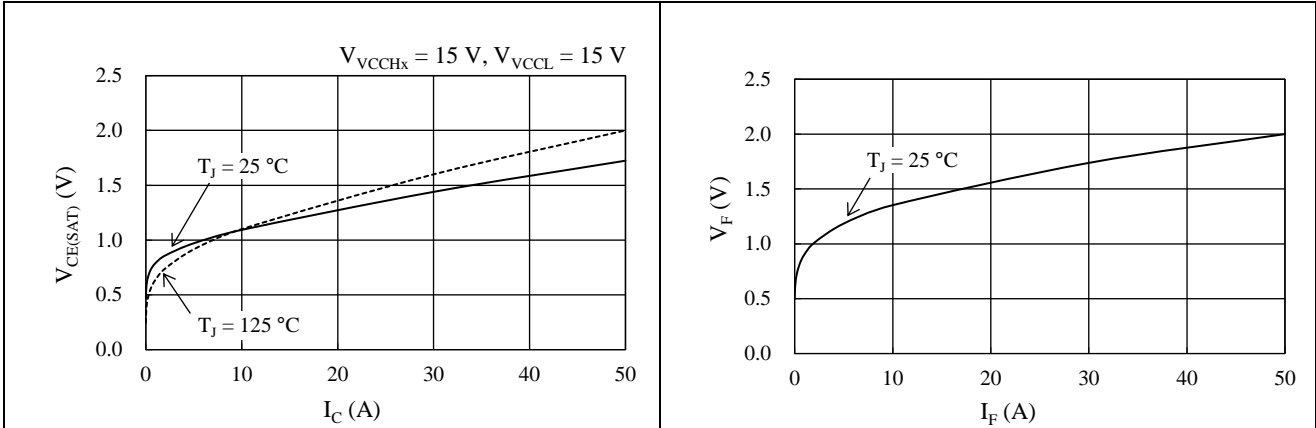


Figure 16-2. IGBT  $V_{CE(SAT)}$  vs.  $I_C$

Figure 16-3. Freewheeling Diode  $V_F$  vs.  $I_F$

16.2.2. Switching Loss Curves

Conditions: P pin voltage = 300 V, half-bridge circuit with inductive load.  
Switching Loss, E, is the sum of turn-on loss and turn-off loss.

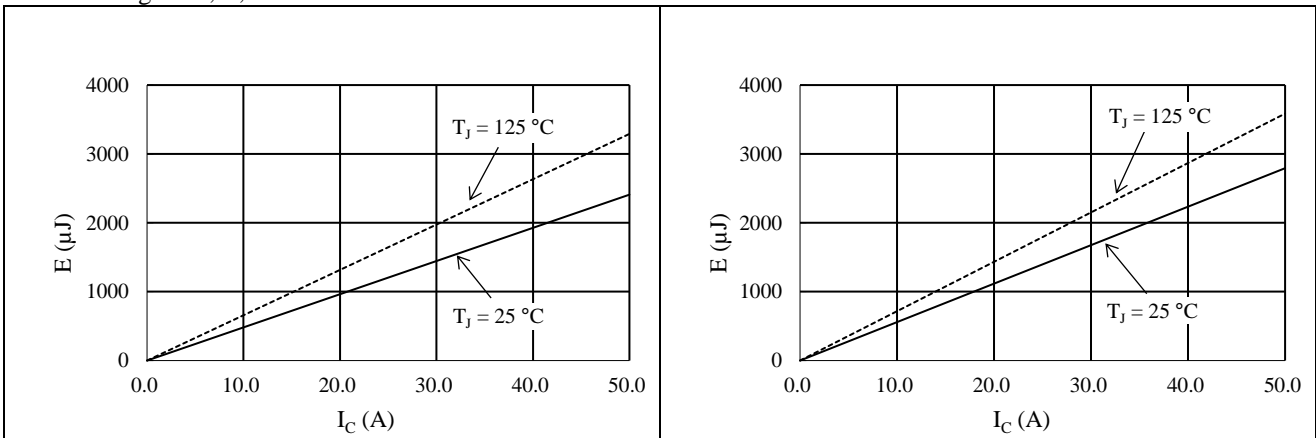


Figure 16-4. High-side Switching Loss

Figure 16-5. Low-side Switching Loss

**16.3. Allowable Effective Current Curves**

The following curves represent allowable effective currents in 3-phase sine-wave PWM driving with parameters such as maximum  $V_{CE(SAT)}$  and maximum switching losses.

Operating conditions: P pin input voltage,  $V_{P(DC)} = 300$  V; VCCHx pin input voltage,  $V_{VCCHx} = 15$  V; VCCL pin input voltage,  $V_{VCCL} = 15$  V; modulation index,  $M = 1.0$ ; junction temperature,  $T_J = 150$  °C; output frequency = 60 Hz.

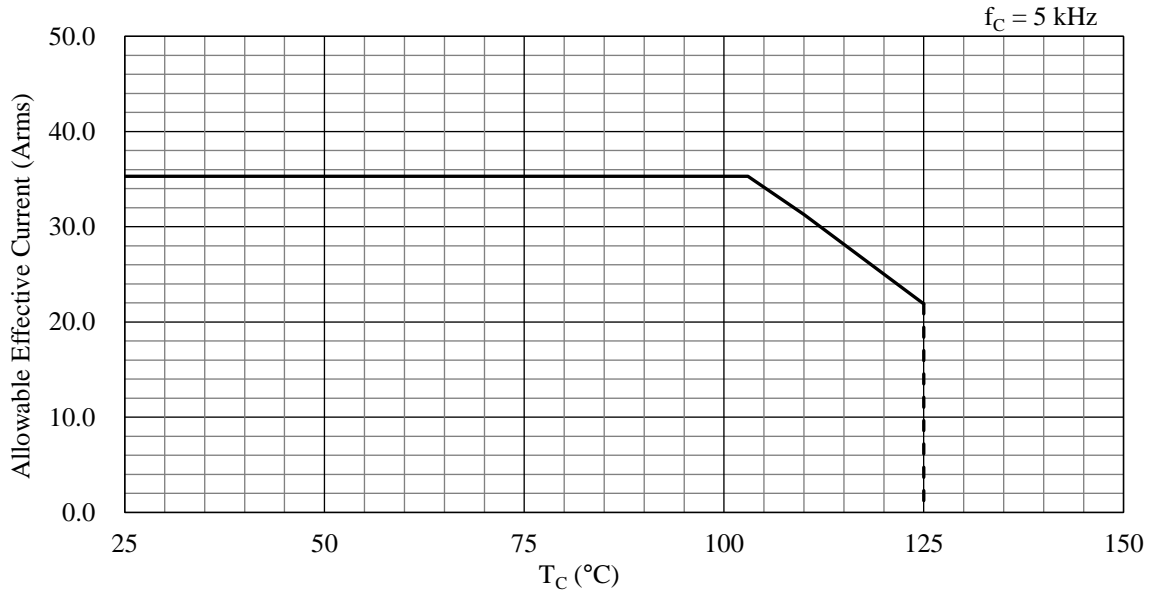


Figure 16-6. Allowable Effective Current ( $f_c = 5$  kHz)

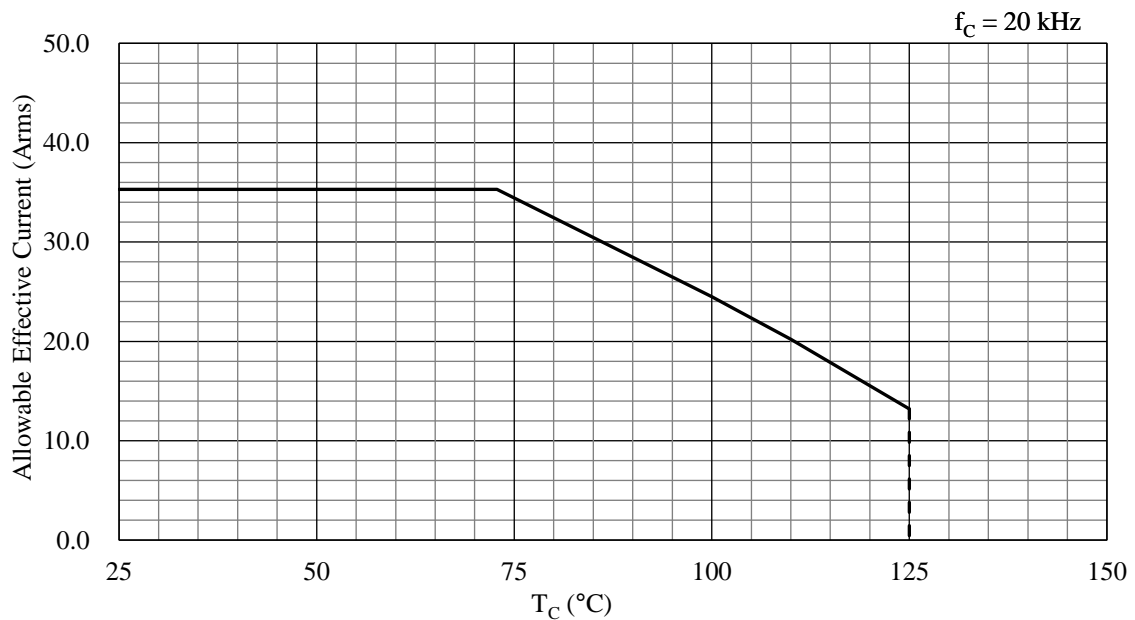


Figure 16-7. Allowable Effective Current ( $f_c = 20$  kHz)

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