Power MOSFET Module

SHD4111

Data Sheet

Description

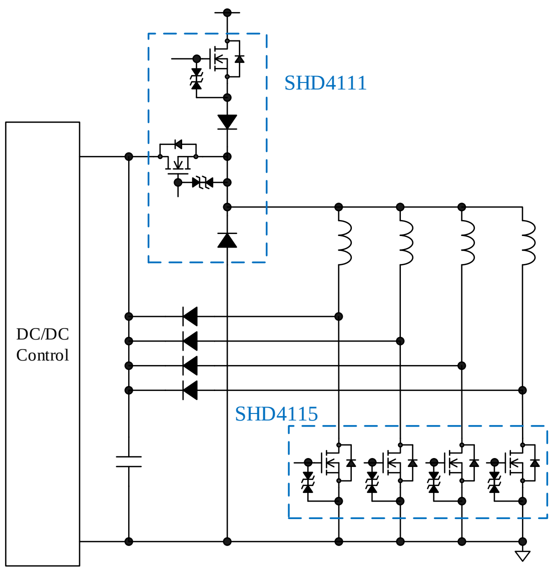
The SHD4111 includes four elements (two fast recovery diodes, two N-channel power MOSFETs) in its small HSON package. The internal power MOSFETs have Zener diodes between gates and sources, thus requiring no externally clamped circuit for an injection coil drive circuit. Supplied in a low thermal resistance package, the product achieves high performance in heat dissipation. In addition, its HSON package employs a wettable flank structure, with the pin tips plated and the case resin around the pins grooved. This achieves higher reliability in mounting.

Features

- High Reliability Achieved
- Automotive Requirements Satisfied
- AEC-Q101 Qualified
- Bare Lead Frame: Pb-free (RoHS Compliant)
- Wettable Flank HSON Package
- Case Resin around the Pins Grooved
- Built-in Zener Diodes between Gates and Sources
- Specifications
  D1, D2: Fast Recovery Diodes (200 V, 5 A)
  Q1: N-channel Power MOSFET (100 V, 10 A)
  Q2: N-channel Power MOSFET (40 V, 10 A)

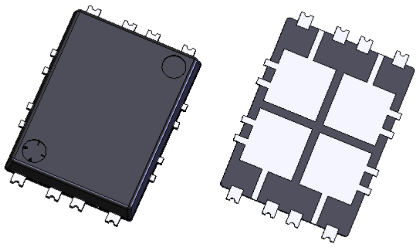
Typical Application

- **Solenoid Injection System**



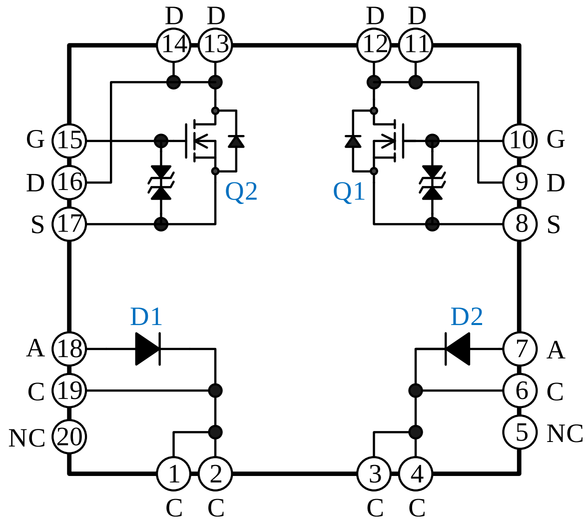
Package

- HSON-20



Not to scale

Internal Schematic Diagram



A: Diode Anode
C: Diode Cathode
D: Power MOSFET Drain
S: Power MOSFET Source
G: Power MOSFET Gate
NC: No Connection

Application

- Injection Coil Driver Circuits

Contents

1. Absolute Maximum Ratings (Common to All Elements)

Parameter	Symbol	Conditions	Rating	Unit
Power Dissipation	P_D	T_C = 25 °C, all elements operating; mounted on an FR4 board (26 mm × 36 mm × 1.66 mm); see Figure 1-1	1.7	W
		T_C = 25 °C, all elements operating; with an infinite heatsink; see Figure 1-1	80	W
Junction Temperature	T_J		150	°C
Storage Temperature	T_{STG}		−55 to 150	°C

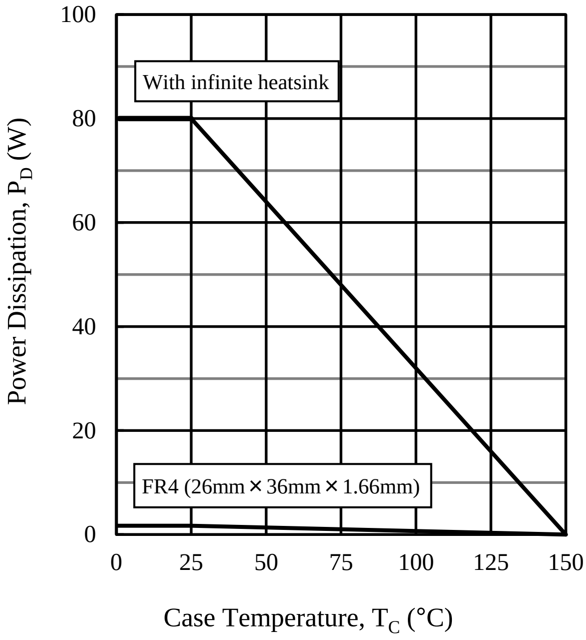


Figure 1-1. P_D vs. T_C (All Elements Operating)

2. Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Junction-to-Case Thermal Resistance	$R_{\theta JC}$	T_C = 25 °C; with an infinite heatsink	—	—	6.25	°C/W

3. Absolute Maximum Ratings and Electrical Characteristics

3.1. D1, D2 (200 V, 5 A Fast Recovery Diodes)

3.1.1. Absolute Maximum Ratings

Unless otherwise specified, T_A = 25 °C.

Parameter	Symbol	Conditions	Rating	Unit
Nonrepetitive Peak Reverse Voltage	V_{RSM}		200	V
Repetitive Peak Reverse Voltage	V_{RM}		200	V
Average Forward Current	$I_{F(AV)}$		5	A
Surge Forward Current	I_{FSM}	t ≤ 30 µs, duty cycle ≤ 1%	30	A
I^2t Limiting Value	I^2t		4.5	A^2s

3.1.2. Electrical Characteristics

Unless otherwise specified, T_A = 25 °C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Voltage Drop	V_F	T_J = 25 °C, I_F = 5 A	—	—	1	V
Reverse Leakage Current	I_R	$V_R = V_{RM}$	—	—	50	µA
Reverse Leakage Current under High Temperature	$H{\cdot}I_R$	$V_R = V_{RM}$, T_J = 150 °C	—	—	300	µA
Reverse Recovery Time	t_{rr}	$I_F = I_{RP}$ = 100 mA, 90% recovery point, T_J = 25 °C	—	—	50	ns

3.1.3. Characteristic Curves

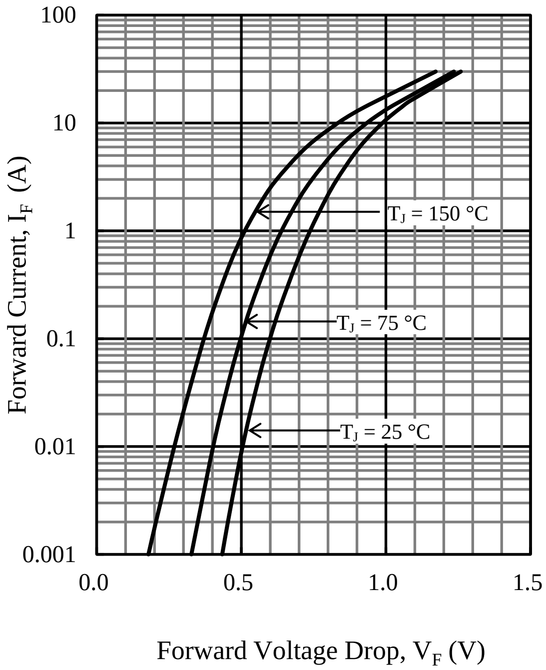


Figure 3-1. D1, D2 Typical Characteristics: I_F vs. V_F

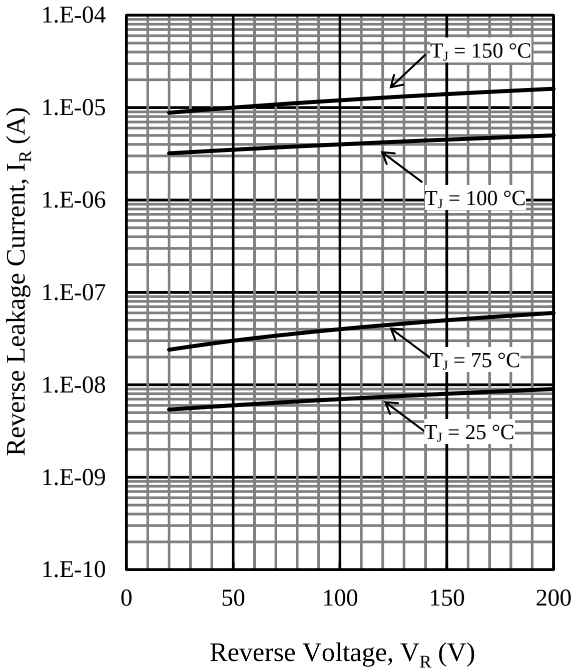


Figure 3-2. D1, D2 Typical Characteristics: I_R vs. V_R

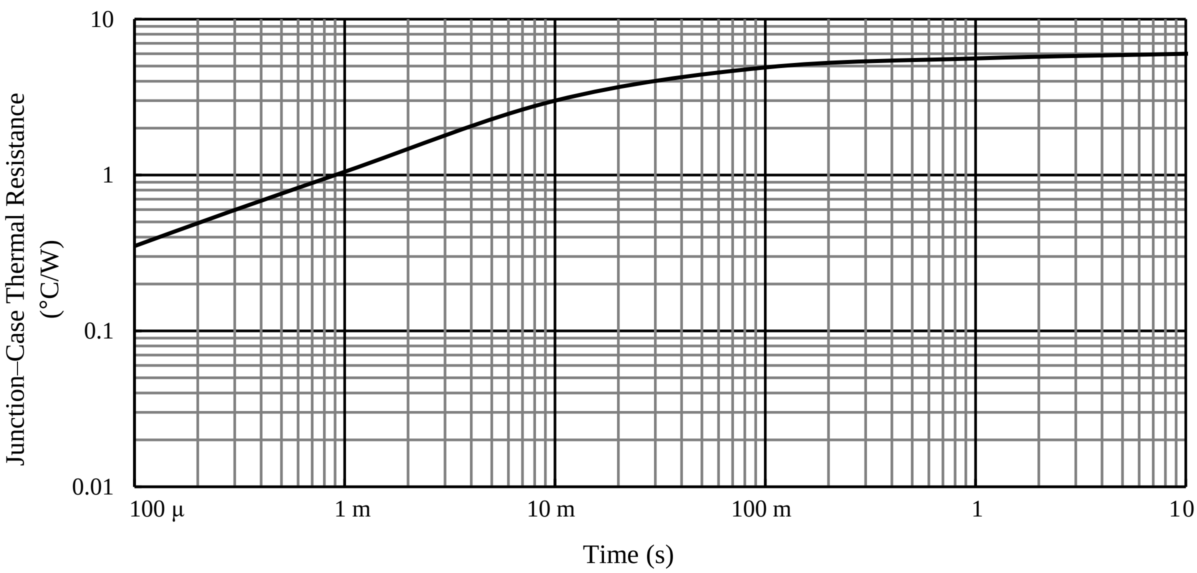


Figure 3-3. D1, D2 Transient Thermal Resistance Characteristic (Single Pulse, T_C = 25 °C)

3.2. Q1 (100 V, 10 A Power MOSFET)

3.2.1. Absolute Maximum Ratings

Unless otherwise specified, T_A = 25 °C.

Parameter	Symbol	Conditions	Rating	Unit
Drain-to-Source Voltage	V_{DS}		100	V
Gate-to-Source Voltage	V_{GS}		±20	V
Continuous Drain Current	I_D	T_C = 25 °C	10	A
Pulsed Drain Current	I_{DM}	t ≤ 30 µs, duty cycle ≤ 1 %	30	A
Avalanche Energy	E_{AS}	Single pulse, V_{DD} = 14 V, L = 1.0 mH, I_D = 10 A, unclamped, R_G = 50 Ω; see Figure 3-32	62.5	mJ
Avalanche Current	I_{AS}		10	A
Maximum Drain-to-Source dv/dt	dv/dt1	V_{DD} = 14 V, L = 1.08 mH, I_D = 10 A, unclamped, R_G = 50 Ω; see Figure 3-32	0.6	V/ns
Maximum Diode Recovery dv/dt	dv/dt2	See Figure 3-33	5	V/ns
Maximum Diode Recovery di/dt	di/dt	See Figure 3-33	100	A/µs

3.2.2. Electrical Characteristics

Unless otherwise specified, T_A = 25 °C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA, V_{GS} = 0 V	100	—	—	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	—	—	100	µA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS} = ±15 V	—	—	± 10	µA
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 5 A	9	—	—	S
Static Drain-to-Source On-resistance	$R_{DS(ON)}$	I_D = 5 A, V_{GS} = 10 V	—	38	50	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	2200	—	pF
Output Capacitance	C_{oss}		—	210	—	
Reverse Transfer Capacitance	C_{rss}		—	110	—	
Total Gate Charge	Q_G	V_{DD} = 50 V, I_D = 5 A, V_{GS} = 10 V, R_L = 10 Ω	—	45	—	nC
Gate-to-Source Charge	Q_{GS}		—	6	—	
Gate-to-Drain Charge	Q_{GD}		—	10	—	
Turn-on Delay Time	$t_{d(ON)}$	V_{DD} = 50 V, I_D = 5 A, V_{GS} = 10 V, R_G = 20 Ω, R_L = 10 Ω; see Figure 3-34	—	30	—	ns
Turn-on Rise Time	t_r		—	40	—	
Turn-off Delay Time	$t_{d(OFF)}$		—	160	—	
Turn-off Fall Time	t_f		—	80	—	
Source-to-Drain Diode Forward Voltage Drop	V_{SD}	I_S = 10 A, V_{GS} = 0 V	—	—	1.2	V
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	I_S = 10 A, di/dt = 100 A/µs; see Figure 3-33	—	50	—	ns

3.2.3. Derating Curves

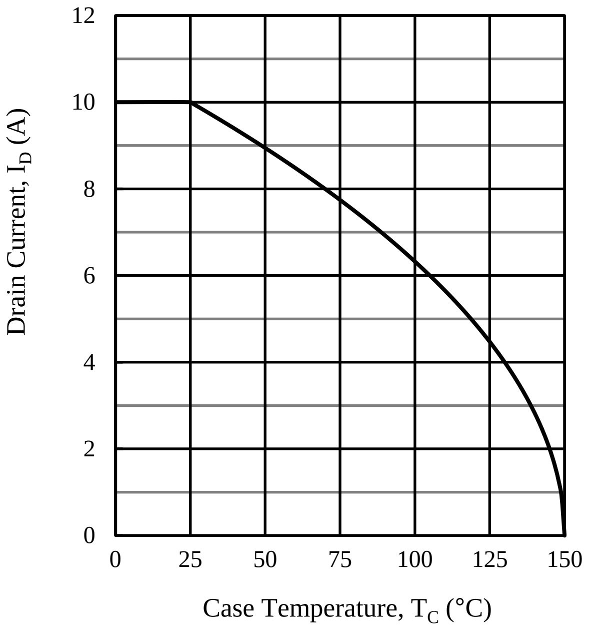


Figure 3-4. Q1 I_D vs. T_C

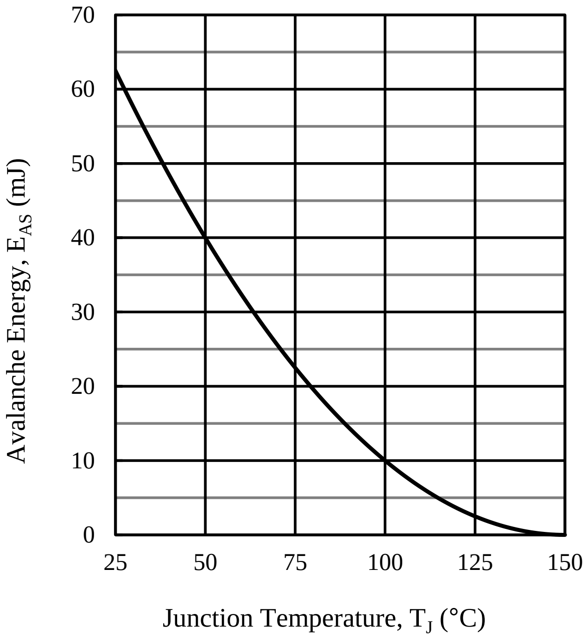


Figure 3-5. Q1 E_{AS} vs. T_J (Single Pulse)

3.2.4. Characteristic Curves

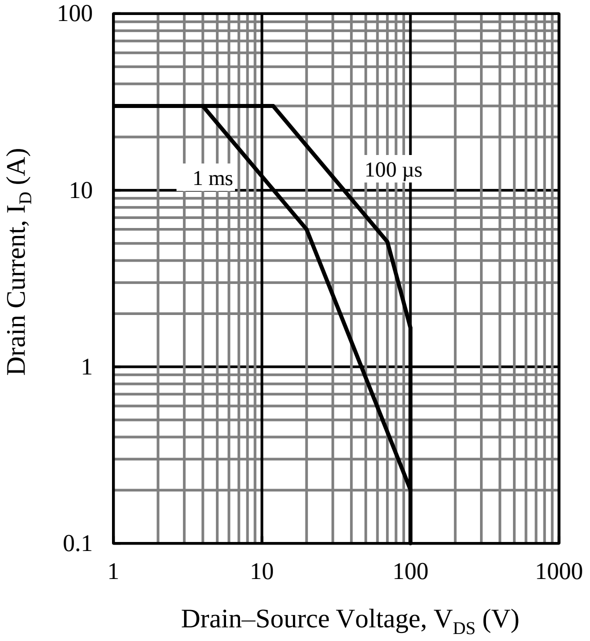


Figure 3-6. Q1 Safe Operating Area
(Single Pulse, T_J = 25 °C)

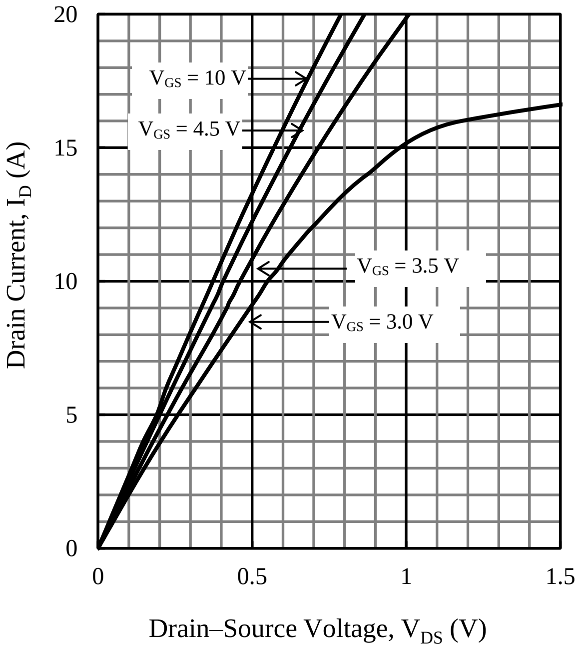


Figure 3-7. Q1 Typical Characteristics:
I_D vs. V_{DS} (T_J = 25 °C)

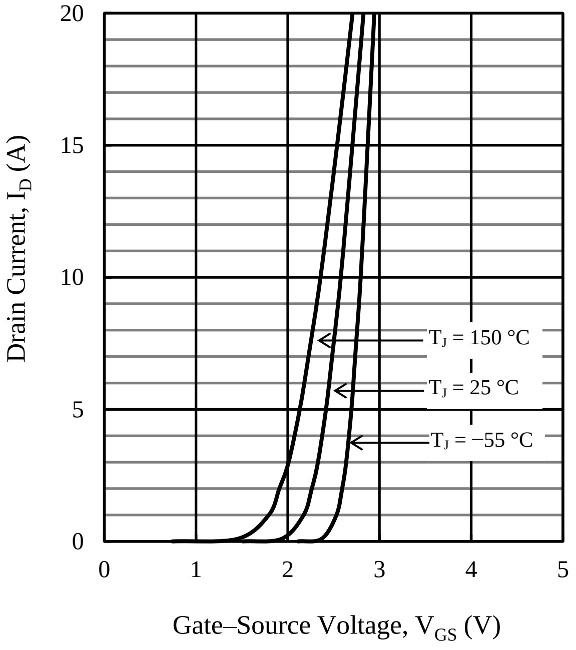


Figure 3-8. Q1 Typical Characteristics:
I_D vs. V_{GS} (V_{DS} = 10 V)

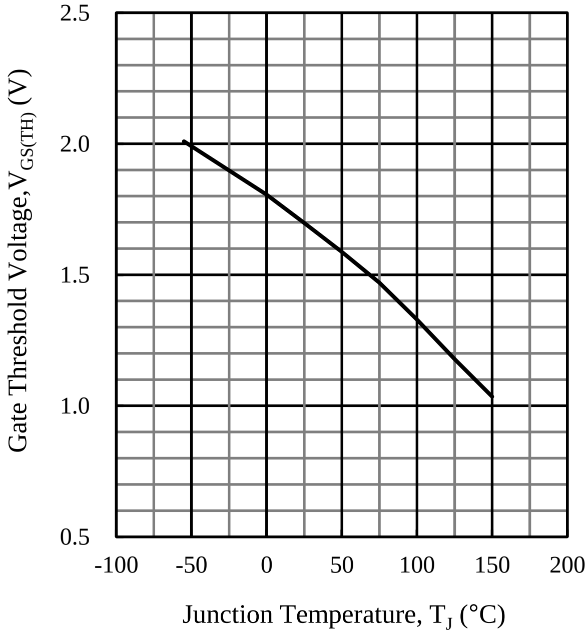


Figure 3-9. Q1 Typical Characteristic:
$V_{GS(TH)}$ vs. T_J (V_{DS} = 10 V, I_D = 1 mA)

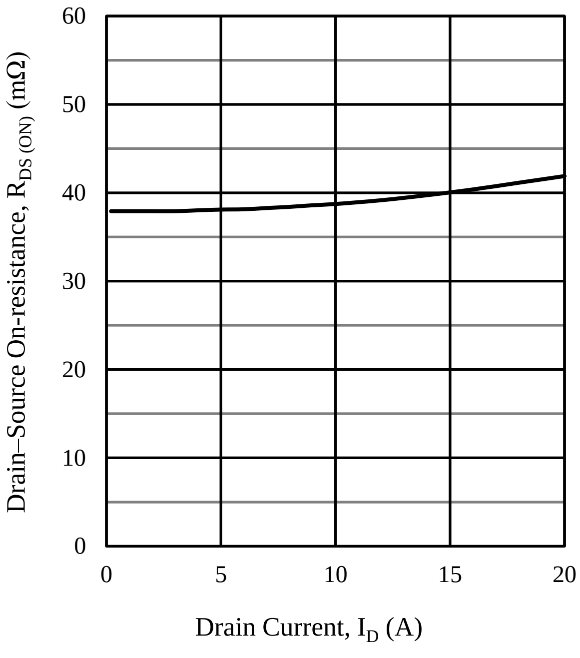


Figure 3-10. Q1 Typical Characteristic:
$R_{DS(ON)}$ vs. I_D (V_{GS} = 10 V, T_J = 25 °C)

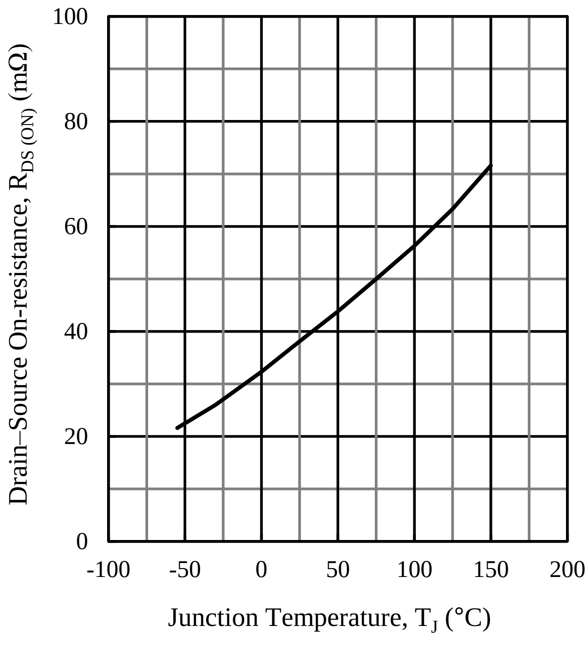


Figure 3-11. Q1 Typical Characteristic:
$R_{DS(ON)}$ vs. T_J (V_{GS} = 10 V, I_D = 5 A)

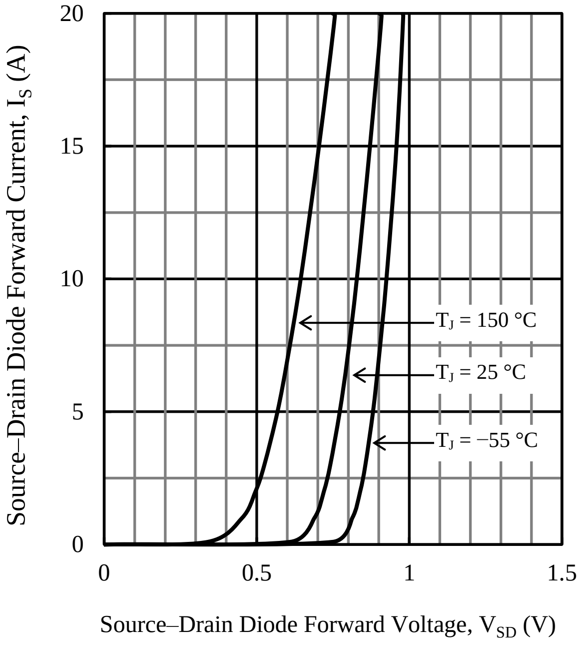


Figure 3-12. Q1 Typical Characteristics: I_S vs. V_{SD} (V_{GS} = 0 V)

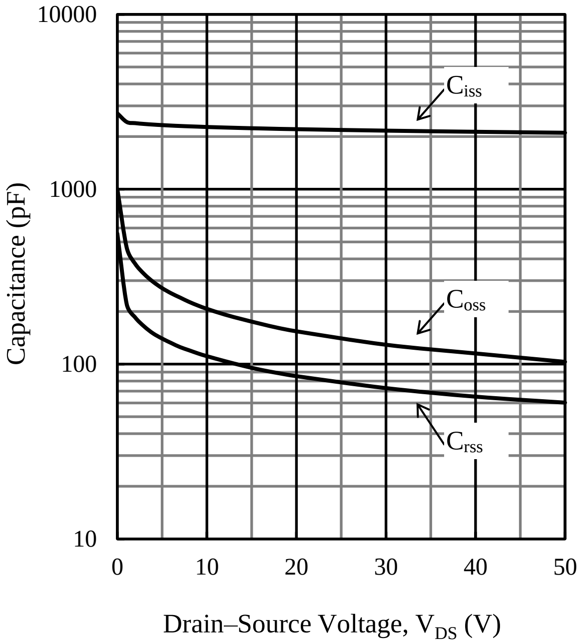


Figure 3-13. Q1 Typical Characteristics: Capacitance vs. V_{DS} (f = 1 MHz, V_{GS} = 0 V)

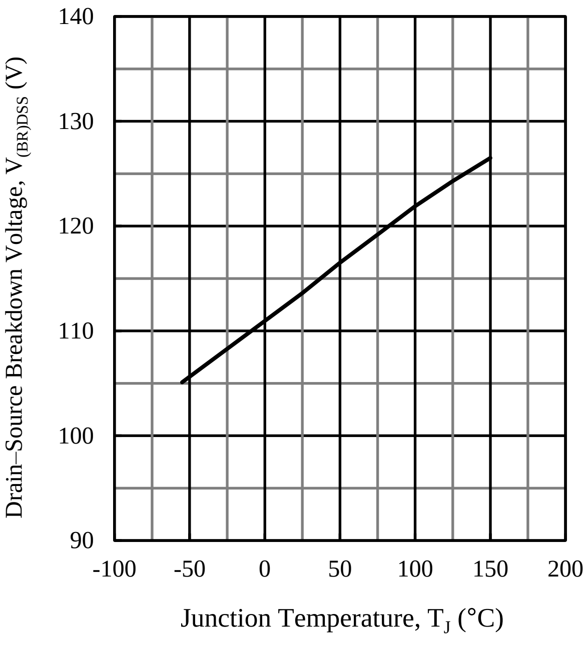


Figure 3-14. Q1 Typical Characteristic: Q1 $V_{(BR)DSS}$ vs. T_J (I_D = 10 mA, V_{GS} = 0 V)

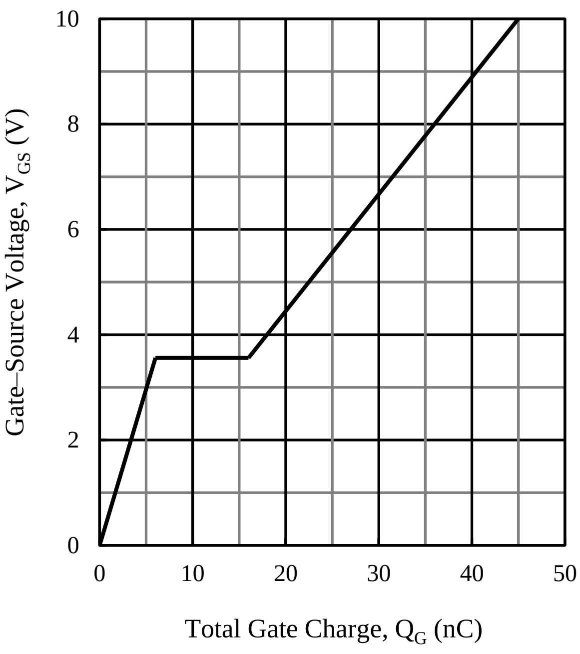


Figure 3-15. Q1 Typical Characteristic: V_{GS} vs. Q_G (I_D = 5 A, $V_{DD} \approx$ 50 V)

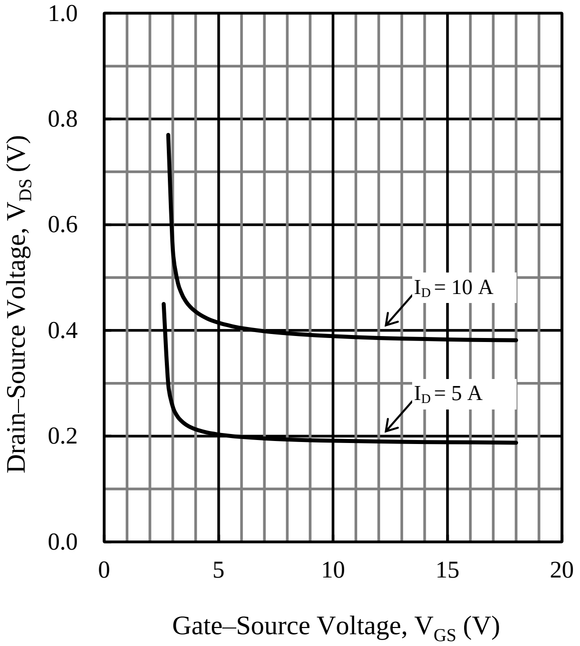


Figure 3-16. Q1 Typical Characteristics: V_{DS} vs. V_{GS} (V_{DS} = 10 V)

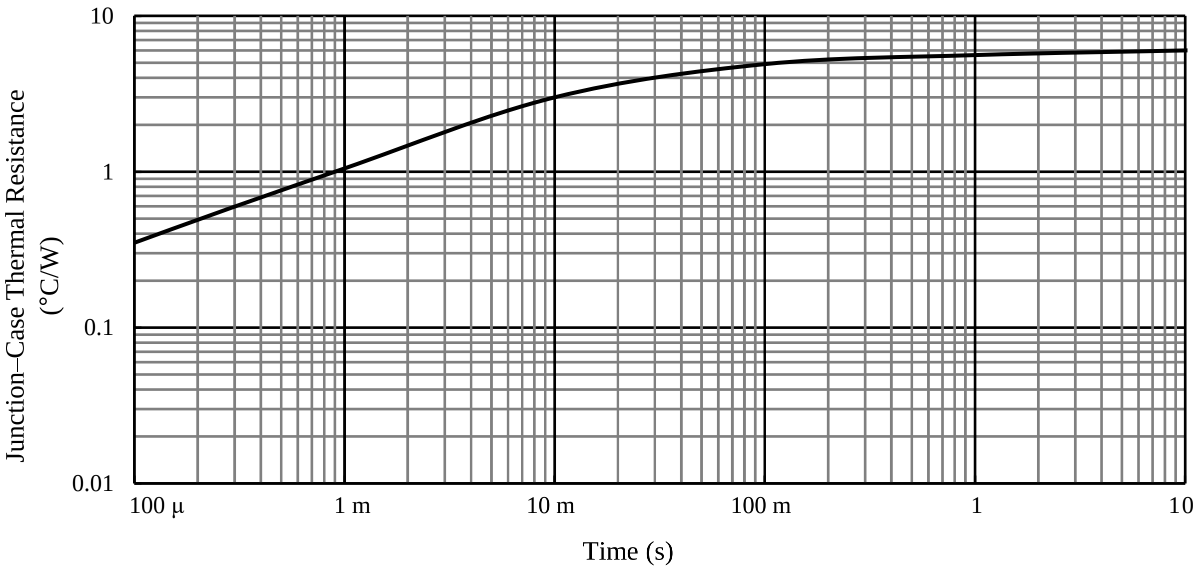


Figure 3-17. Q1 Transient Thermal Resistance Characteristic (Single Pulse, Single Pulse, V_{DS} < 10 V)

3.3. Q2 (40 V, 10 A Power MOSFET)

3.3.1. Absolute Maximum Ratings

Unless otherwise specified, T_A = 25 °C.

Parameter	Symbol	Conditions	Rating	Unit
Drain-to-Source Voltage	V_{DS}		40	V
Gate-to-Source Voltage	V_{GS}		±20	V
Continuous Drain Current	I_D	T_C = 25 °C	10	A
Pulsed Drain Current	I_{DM}	t ≤ 30 µs, duty cycle ≤ 1 %	30	A
Avalanche Energy	E_{AS}	Single pulse, V_{DD} = 14 V, L = 0.4 mH, I_D = 10 A, unclamped, R_G = 50 Ω; see Figure 3-32	30.5	mJ
Avalanche Current	I_{AS}		10	A
Maximum Drain-to-Source dv/dt	dv/dt1	V_{DD} = 14 V, L = 0.4 mH, I_D = 10 A, unclamped, R_G = 50 Ω; see Figure 3-32	0.2	V/ns
Maximum Diode Recovery dv/dt	dv/dt2	See Figure 3-33	2	V/ns
Maximum Diode Recovery di/dt	di/dt	See Figure 3-33	100	A/µs

3.3.2. Electrical Characteristics

Unless otherwise specified, T_A = 25 °C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA, V_{GS} = 0 V	40	—	—	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 40V, V_{GS} = 0 V	—	—	100	µA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS} = ±15 V	—	—	± 10	µA
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 5 A	5	—	—	S
Static Drain-to-Source On-resistance	$R_{DS(ON)}$	I_D = 5 A, V_{GS} = 10 V	—	15	21	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	1200	—	pF
Output Capacitance	C_{oss}		—	310	—	
Reverse Transfer Capacitance	C_{rss}		—	170	—	
Total Gate Charge	Q_G	V_{DD} = 20 V, I_D = 5 A, V_{GS} = 10 V, R_L = 4 Ω	—	25	—	nC
Gate-to-Source Charge	Q_{GS}		—	3	—	
Gate-to-Drain Charge	Q_{GD}		—	6	—	
Turn-on Delay Time	$t_{d(ON)}$	V_{DD} = 20 V, I_D = 5 A, V_{GS} = 10 V, R_G = 20 Ω, R_L = 4 Ω; see Figure 3-34	—	15	—	ns
Turn-on Rise Time	t_r		—	35	—	
Turn-off Delay Time	$t_{d(OFF)}$		—	100	—	
Turn-off Fall Time	t_f		—	50	—	
Source-to-Drain Diode Forward Voltage Drop	V_{SD}	I_S = 10 A, V_{GS} = 0 V	—	—	1.2	V
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	I_S = 10 A, di/dt = 100 A/µs; see Figure 3-33	—	50	—	ns

3.3.3. Derating Curves

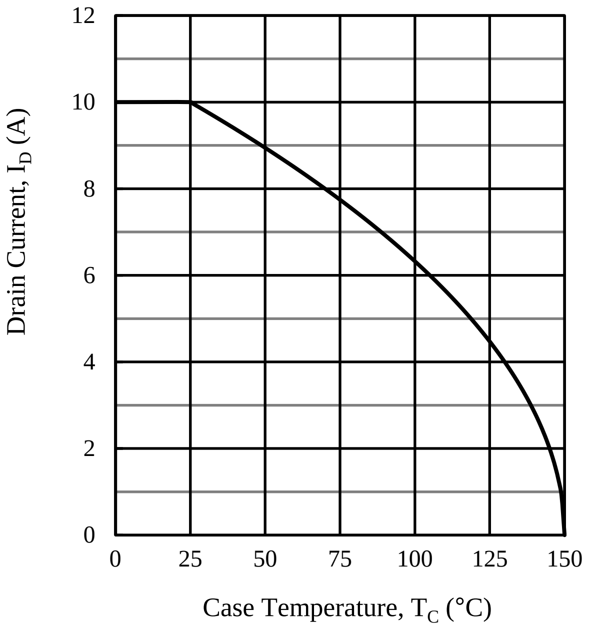


Figure 3-18. Q2 I_D vs. T_C

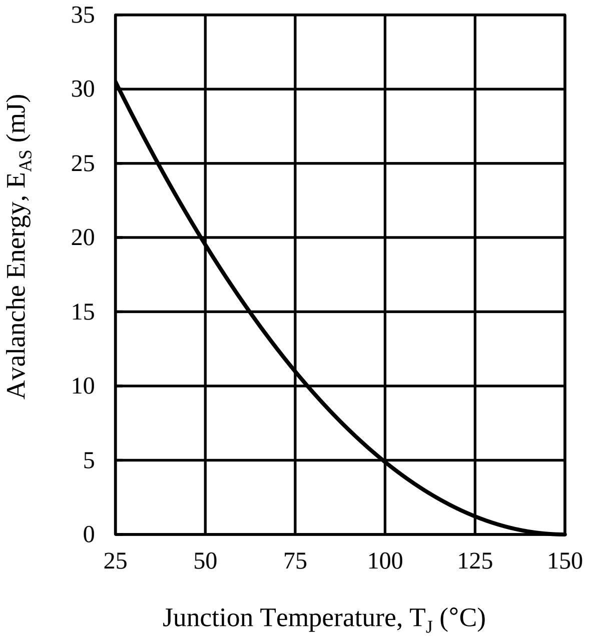


Figure 3-19. Q21 E_{AS} vs. T_J (Single Pulse)

3.3.4. Characteristic Curves

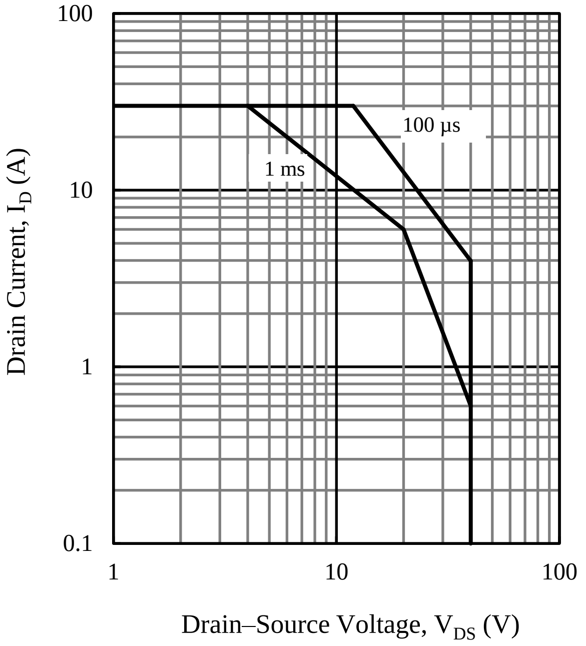


Figure 3-20. Q2 Safe Operating Area (Single Pulse, $T_J = 25$ °C)

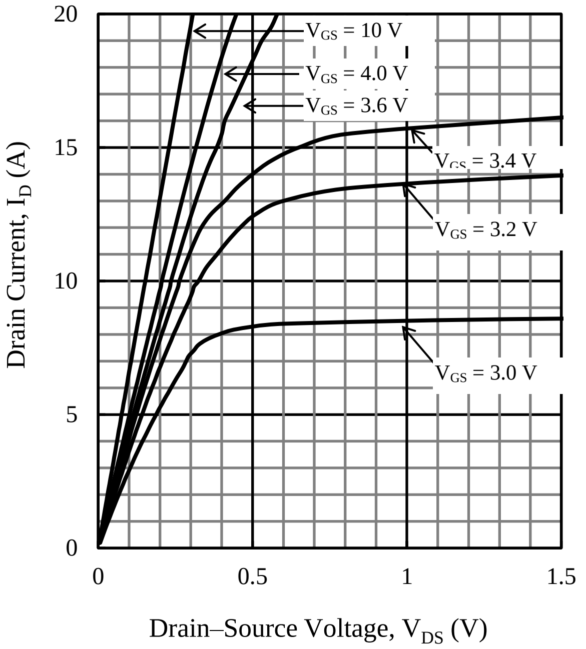


Figure 3-21. Q2 Typical Characteristics: Q2 I_D vs. V_{DS} ($T_J = 25$ °C)

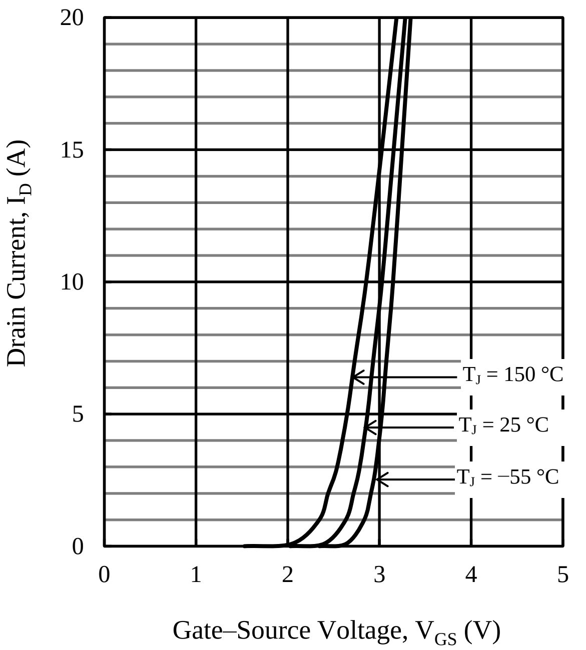


Figure 3-22. Q2 Typical Characteristics: I_D vs. V_{GS} ($V_{DS} = 10$ V)

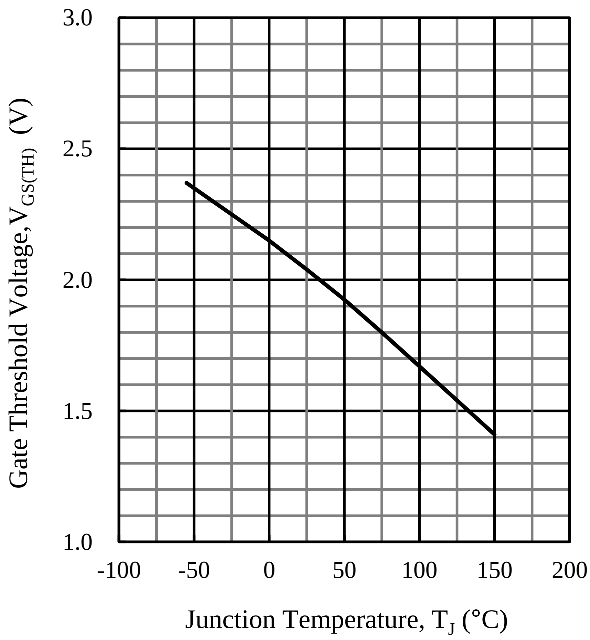


Figure 3-23. Q2 Typical Characteristic: $V_{GS(TH)}$ vs. T_J ($V_{DS} = 10$ V, $I_D = 1$ mA)

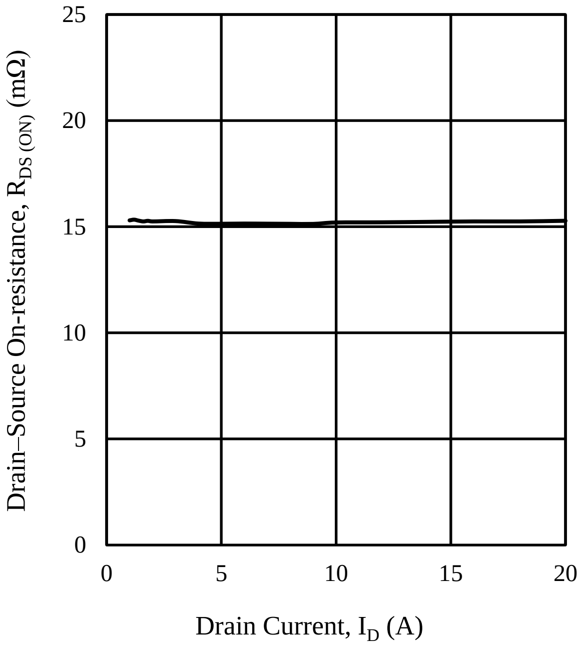


Figure 3-24. Q2 Typical Characteristic:
$R_{DS(ON)}$ vs. I_D (V_{GS} = 10 V, T_J = 25 °C)

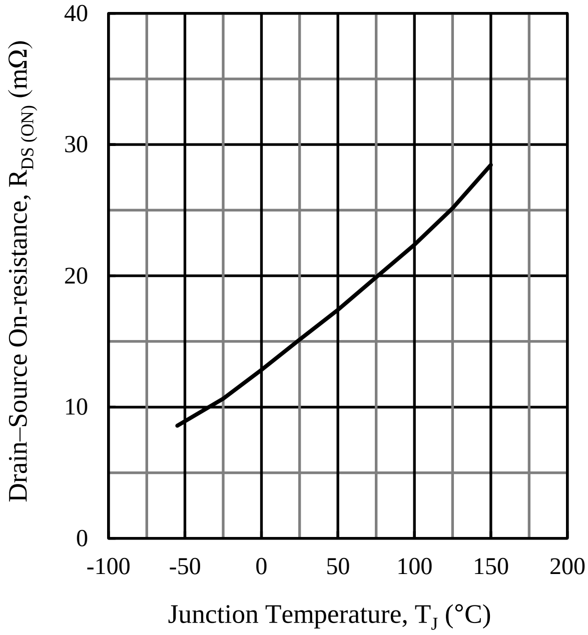


Figure 3-25. Q2 Typical Characteristic:
$R_{DS(ON)}$ vs. T_J (V_{GS} = 10 V, I_D = 5 A)

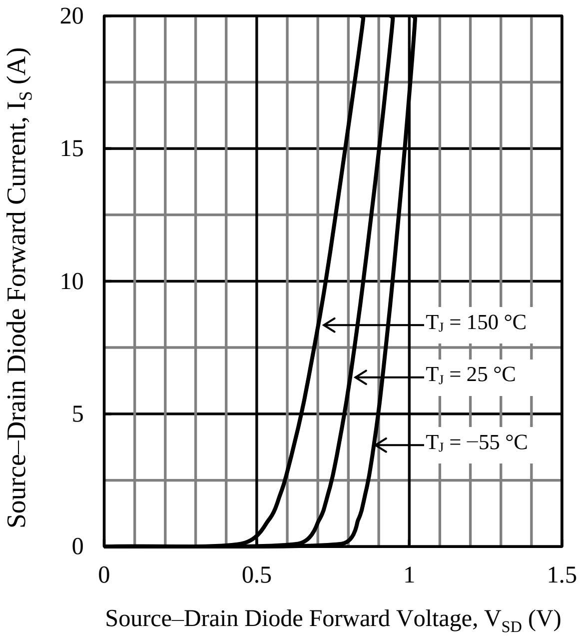


Figure 3-26. Q2 Typical Characteristics:
I_S vs. V_{SD} (V_{GS} = 0 V)

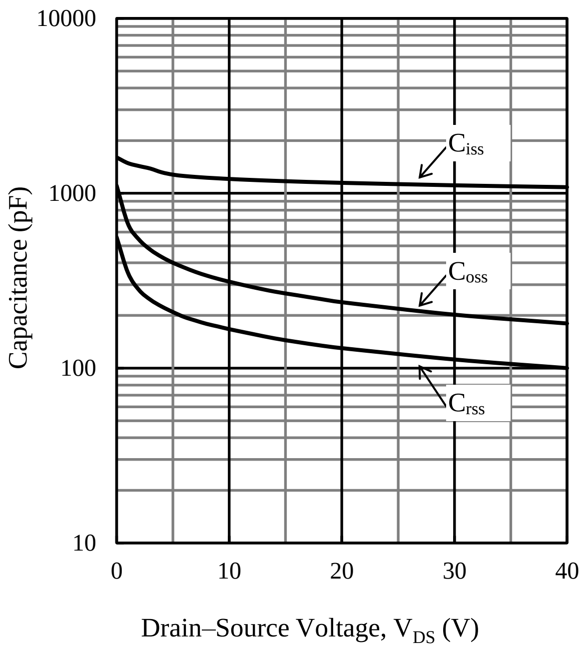


Figure 3-27. Q2 Typical Characteristics:
Capacitance vs. V_{DS} (f = 1 MHz, V_{GS} = 0 V)

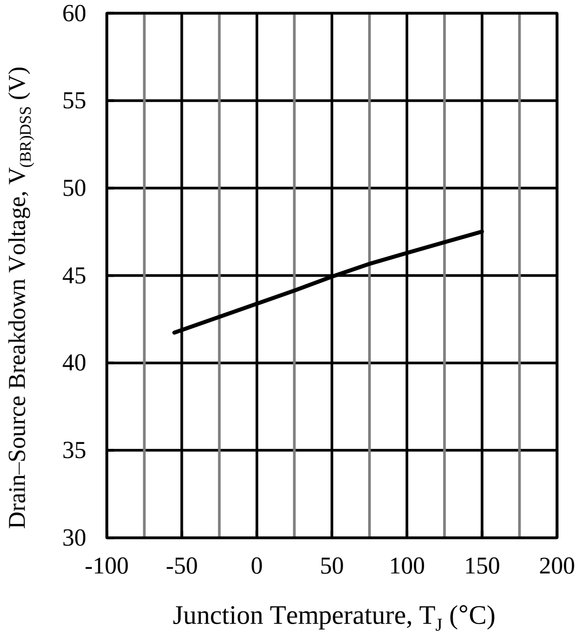


Figure 3-28. Q2 Typical Characteristic:
$V_{(BR)DSS}$ vs. T_J
(I_D = 10 mA, V_{GS} = 0 V)

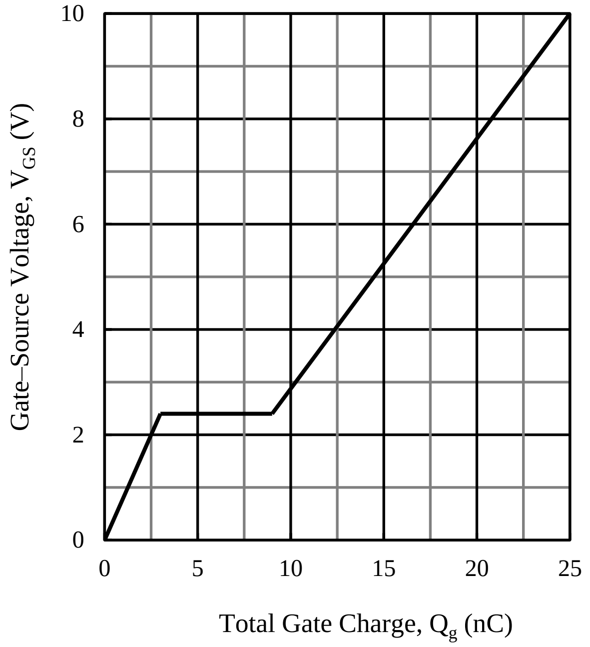


Figure 3-29. Q2 Typical Characteristic:
V_{GS} vs. Q_G (I_D = 5 A, V_{DD} ≈ 20 V)

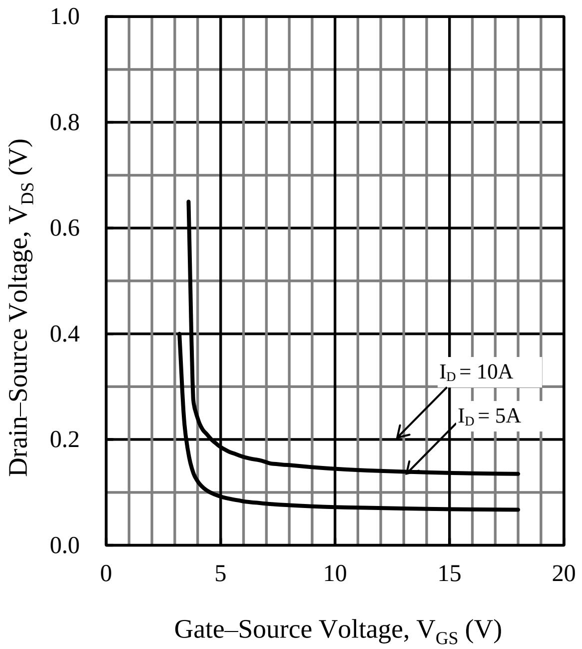


Figure 3-30. Q2 Typical Characteristics:
V_{DS} vs. V_{GS} (V_{DS} = 10 V)

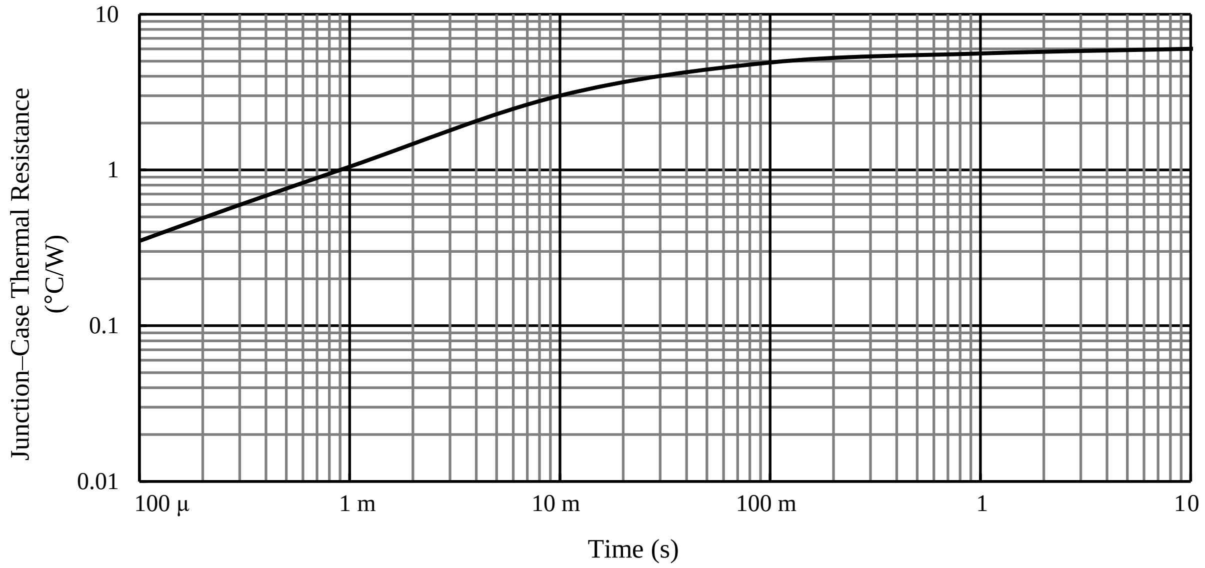
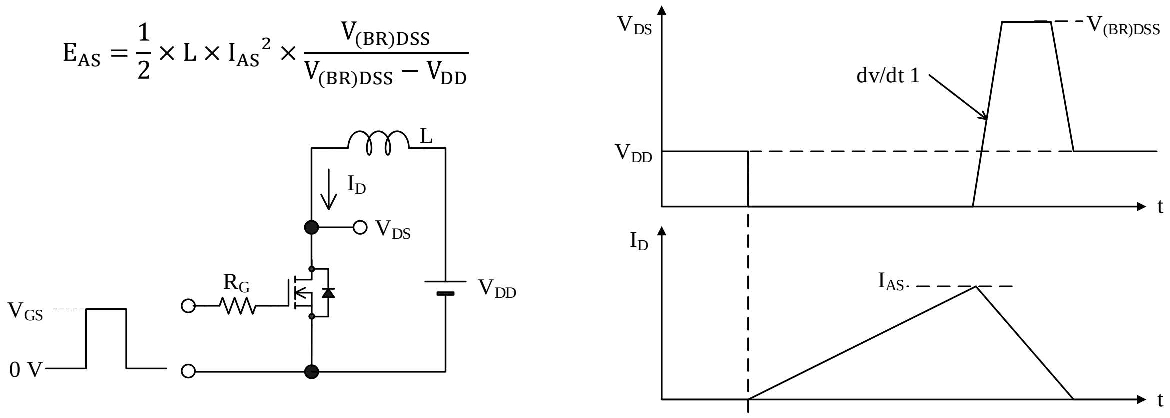


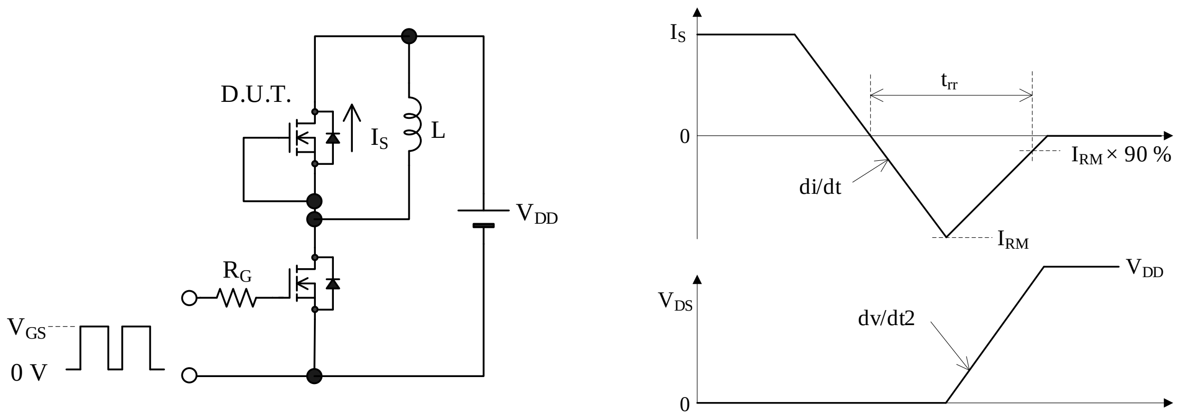
Figure 3-31. Q2 Transient Thermal Resistance Characteristic (Single Pulse, Single Pulse, V_{DS} < 10 V)

$$E_{AS} = \frac{1}{2} \times L \times I_{AS}{}^2 \times \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}$$



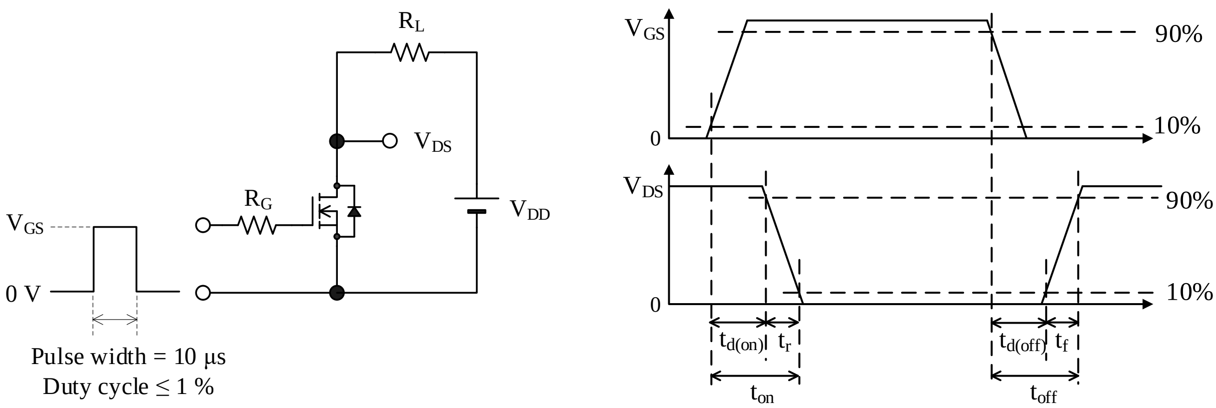
(a) Test Circuit (b) Waveforms

Figure 3-32. Avalanche Energy and dv/dt1 Test



(a) Test Circuit (b) Waveforms

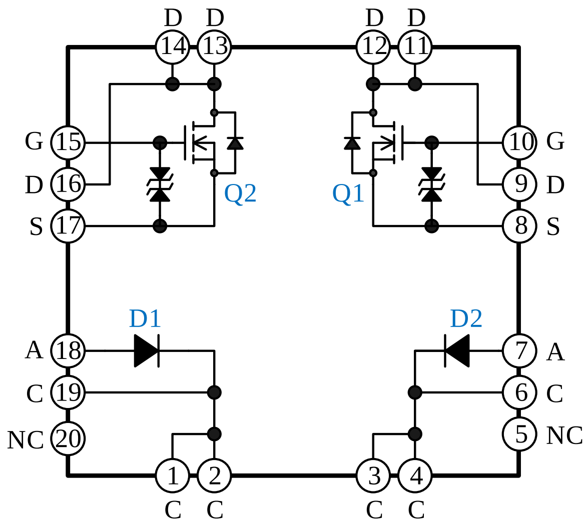
Figure 3-33. Diode Reverse Recovery Time Test



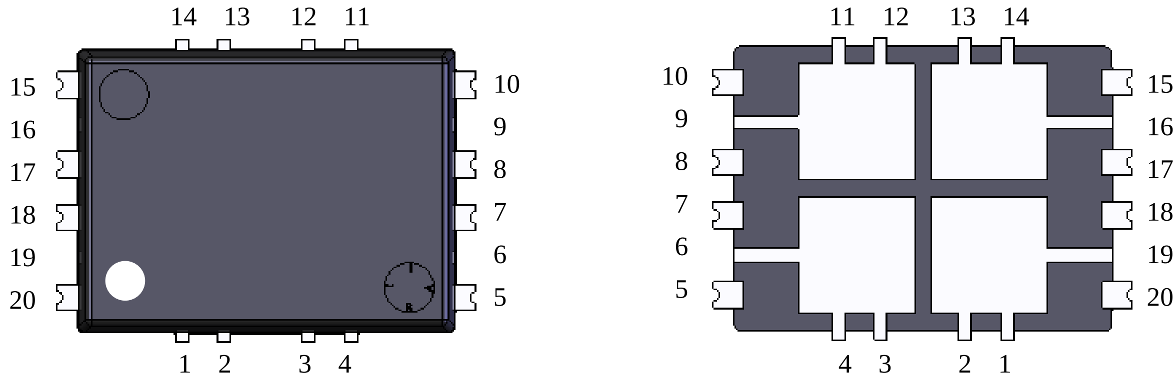
(a) Test Circuit (b) Waveforms

Figure 3-34. Resistive Load Switching Time Test

4. Internal Schematic Diagram



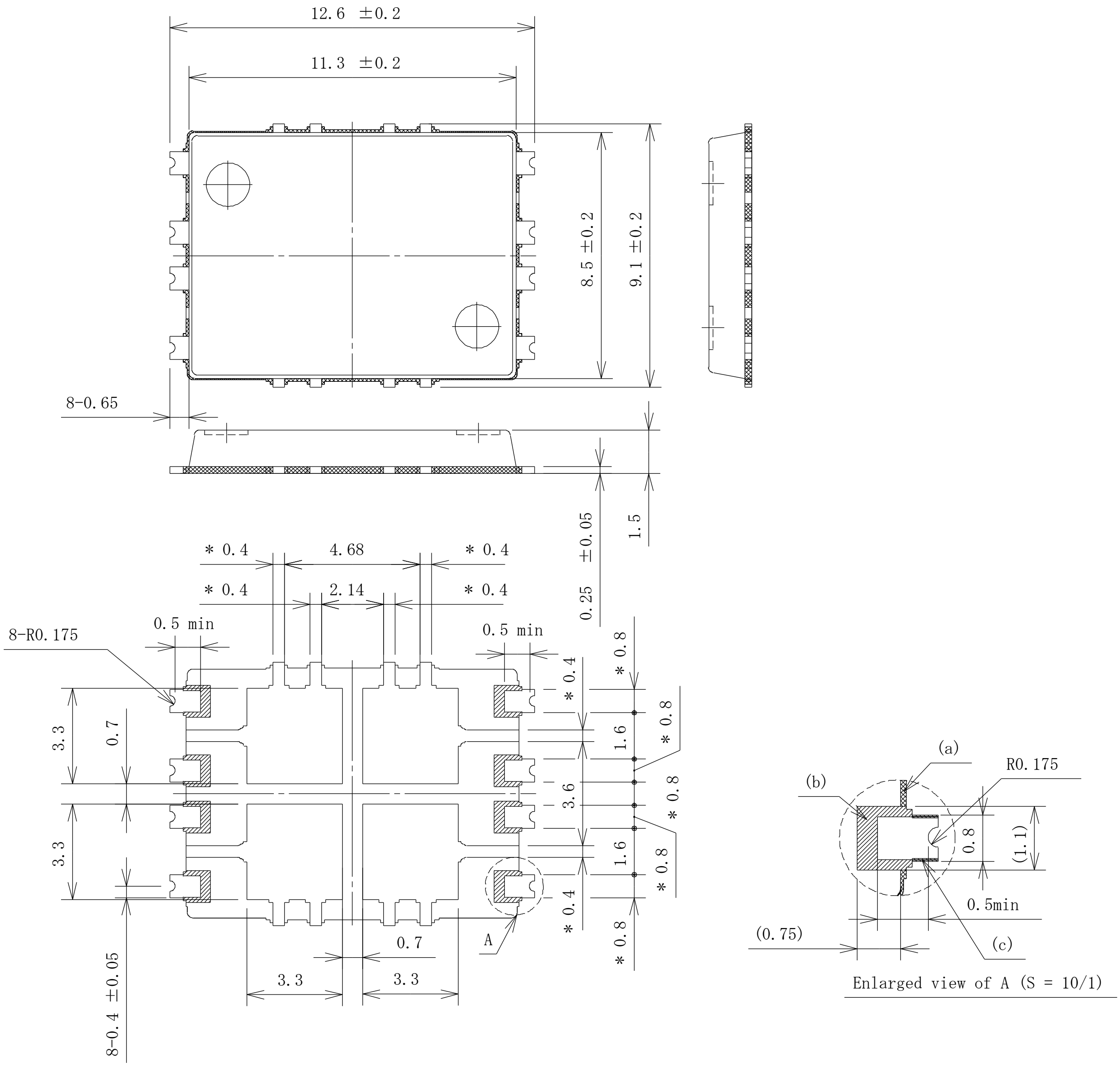
5. Pin Configuration Definitions



Pin Number	Description	Pin Number	Description
1	D1 cathode	11	Q1 drain
2	D1 cathode	12	Q1 drain
3	D2 cathode	13	Q2 drain
4	D2 cathode	14	Q2 drain
5	No connection	15	Q2 gate
6	D2 cathode	16	Q2 drain
7	D2 anode	17	Q2 source
8	Q1 source	18	D1 anode
9	Q1 drain	19	D1 cathode
10	Q1 gate	20	No connection

6. Physical Dimensions

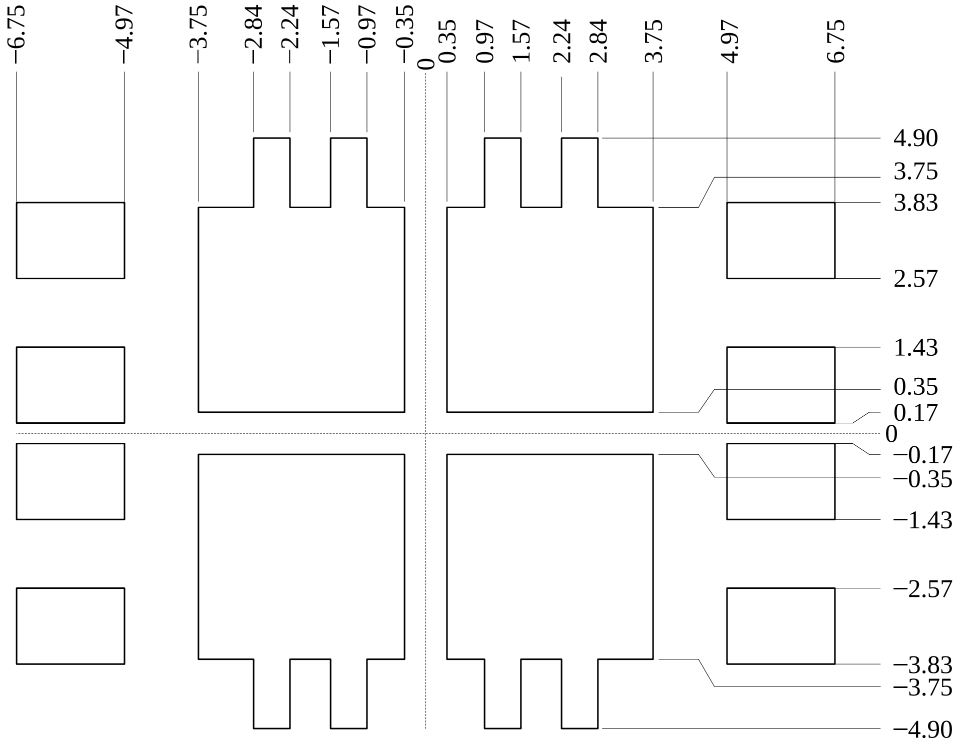
- **HSON-20 Package**



NOTES:

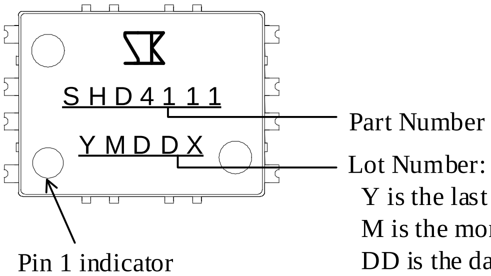
- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)
- Dimensions without tolerances have a tolerance of ±0.1.
- Dimensions with the asterisks do not include any mold flash.
- (a) depicts the area where one or more mold flashes similar in thickness to that of the frame may exist.
- (b) depicts the area where a groove is formed with a target depth of 0.05.
- (c) depicts the area where a frame is crushed with a target width of 0.05.
- Moisture Sensitivity Level 3 (MSL 3)
- When soldering the products, it is required to minimize the working time within the following limits:
  Reflow
    Preheat: 150 °C to 200 °C / 60 s to 120 s
    Solder heating: 255 °C / 30s, 3 times (260 °C peak)
  Soldering iron: 350 °C / 3.5 s, 1 time
- The following pins are not guaranteed to be connected by soldering: 6, 9, 16, and 19.

- **HSON-20 Land Pattern Example**



Unit：mm

7. Marking Diagram



Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
DD is the day of the month (01 to 31)
X is the control number

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