STR-L400 Series Application Note (Rev.1.2)

SANKEN ELECTRIC CO., LTD.

http://www.sanken-ele.co.jp

Contents

!WARNING!

- Sanken reserves the right to make changes without further notice to any products herein in the interest of improvements in the performance, reliability, or manufacturability of its products.
  Before placing order, Sanken advises its customers to obtain the latest version of the relevant information to verify that the information being relied upon is current.
- Application and operation examples described in this application note are provided for a supplementary purpose only.
  Conditions in actual use and variations in additional parts are not considered.
  When using the products herein, the applicability and suitability of such products for the intended purpose or object shall be reviewed at the user's responsibility.
- Application and operation examples described in this application note are given for reference only and Sanken assumes no responsibility for any infringement of industrial property rights, intellectual property rights or any other rights of Sanken, or any third party which may result from its use.
- Although Sanken undertakes to enhance the quality and reliability of its products, the occurrence of failure and defect of semiconductor products at a certain rate is inevitable.
  Users of Sanken products are requested to take, at their own risk, preventative measures including safety design of the equipment or systems against any possible injury, death, fires or damages to society due to device failure or malfunction.
- This publication shall not be reproduced in whole or in part without prior written approval form Sanken.

1. General Descriptions

The STR-L400 series devices comprise an integrated MOSFET and a controller chip for quasi-resonant switching power supply applications. The quasi resonant operation and PRC operation are available in normal operation.

* PRC (Pulse Ratio Control) ---Control system of OFF time fixed and ON time control (Sanken designation)

The SIP10L pin full mold package of low-profile and with creeping distance between high and low voltage of 6.5 mm or longer (lead terminal on substrate) (Sanken's designation: STA package) is used, thus a power supply system with high cost performance, low part count and enhanced protection functions can be easily composed.

2. Features and Product Lineup

Features and Advantages

- SIP10L full mold package (STA10L package, 2.54mm pitch)
  - Creeping distance of 6.5mm of lead terminal on the substrate between high voltage pin and low voltage pin (lead terminal on substrate)
  - Height from substrate: 12mm or lower
  - Most suitable for auxiliary power supply for white goods (home electric appliances)
- Current mode control method
- Built-in oscillator for low frequency operation (it reduces the stress of components at startup or short circuit of output by operating at low frequency (about 20 kHz) of 50μs OFF time until quasi resonant signal is established)
- Quasi resonant operation function
- Input compensation function at overcurrent point (compensation of variation of overcurrent operation is available by adding 3 components)
- Protection functions
  - Overcurrent Protection (OCP) Pulse-by-pulse
  - Overvoltage Protection (OVP) Latch-off *
  - Thermal Shutdown (TSD) Latch-off *
  - *Latch-off: this is an operation to continue the oscillation stop for protection.
- Two-chip structure guarantees avalanche energy (simplified surge absorbing circuit)

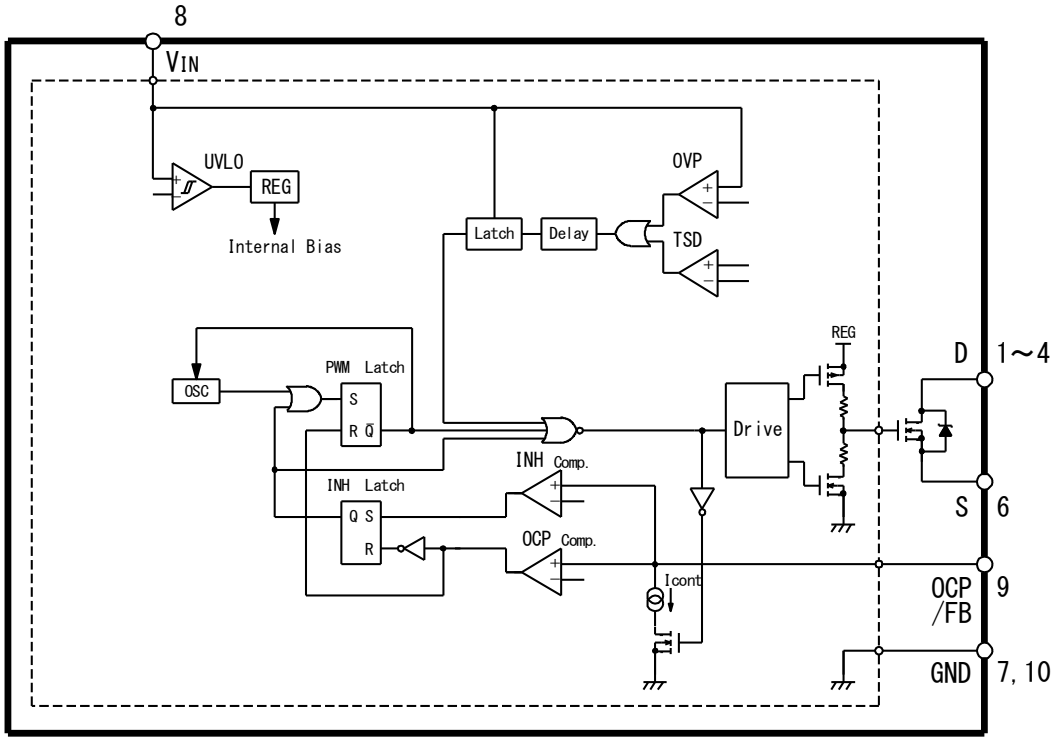
Product Lineup

Product No.	MOSFET V_{DSS}(MIN)	$R_{DS(ON)}$ (Max)	P_{OUT} *1 AC100V/AC230V
STR-L451	650V	3.95Ω	30W / 74W
STR-L472	900V	7.70Ω	－ / 35W

*1: The maximum output power is derived from thermal specifications. The actual output power may be available around 120 - 140% of the above values, respectively, but will be limited by ON duty setting on transformer design or lower output voltage.

3. Functional Block Diagram and Terminal Function

Block Diagram

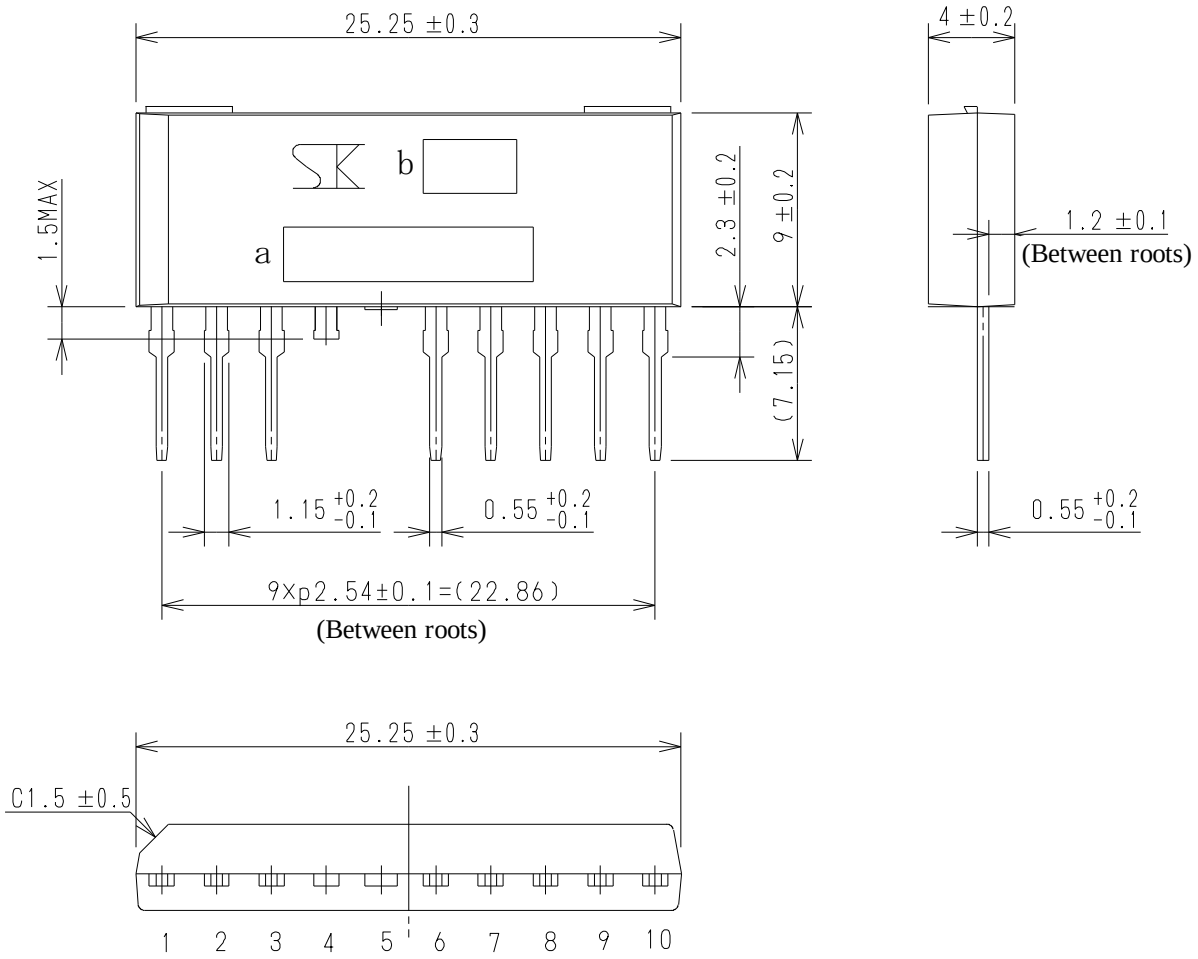


Terminal List Table

Terminal No.	Symbol	Functions
1 - 4	D	MOSFET drain
6	S	MOSFET source
7,10	GND	Ground
8	V_{IN}	Control circuit power supply input
9	OCP/FB	Overcurrent detection signal input / Constant voltage control signal input

4. Package information

- SIP10L (Sanken designation: STA10L)
- The lead forming shown below is No. LF 428



Terminal material: Cu
Terminal processing: Solder dip
Product weight: around 2.6g
Unit: mm
_____shows the spot where the gate burr with the height of 0. 3 mm max. is produced.

a. Type Number
b. Lot Number
1st letter The last digit of year
2nd letter Month
January to September by Arabic number
October by O
November by N
December by D
3rd & 4th letter Day
01 – 31: Arabic Numerical

5. Electrical Characteristics

The following tables provide electrical characteristics for the STR-L400 series. The STR-L472 is used as an example. Refer to the specification of the individual devices for details.

Absolute Maximum Ratings valid at Ta=25°C unless otherwise specified.

Parameter	Terminal	Symbol	Rating	Unit	Note
Drain Current *1	1 – 6	I_{DPeak}	2.7	A	Single pulse
Maximum Switching Current *1	1 – 6	I_{DMAX}	2.7	A	V_{6-10}=0.82V Ta= -20 - +125°C
Avalanche Energy *1	1 – 6	E_{AS}	50	mJ	Single pulse V_{DD}=30V,L=20mH I_{LPeak}= 2.2A
Supply Voltage for Control Circuit	8 – 10	V_{IN}	35	V	
OCP/FB Terminal Voltage	9 – 10	V_{th}	6	V	
Power Dissipation in MOSFET *1	1 – 6	P_{D1}	12	W	With infinite heat sink
			2.5		Without heat sink
Power Dissipation in Control Circuit MIC)	8 – 10	P_{D2}	0.14	W	
Internal Frame Temperature in Operation	—	T_F	-20 - +125	°C	Recommended internal frame temperature T_F= 105°C (Max)
Operating Ambient Temperature	—	T_{OP}	-20 - +125	°C	
Storage Temperature	—	T_{stg}	-40 - +125	°C	
Channel Temperature	—	T_{ch}	+150	°C	

*1 Refer to individual device datasheet for details; value differs among devices.

* Current characteristics are defined based on IC as Sink:+, Source:－.

Electrical Characteristics in MOSFET valid at Ta=25°C unless otherwise specified.

Parameter	Terminal	Symbol	Rating			Unit	Note
			MIN	TYP	MAX		
Drain-source Voltage *2	1 – 6	V_{DSS}	900	—	—	V	
Drain Leakage Current	1 – 6	I_{DSS}	—	—	300	A	
ON Resistance *2	1 – 6	$R_{DS(ON)}$	—	—	7.7	Ω	
Switching Time *2	1 – 6	t_f	—	—	250	ns	
Thermal Resistance *2	—	θ_{ch-F}	—	—	5.05	°C/W	Channel to internal frame

*2 Refer to individual device datasheet for details; value differs among devices.

Control Circuit Electrical Characteristics valid at Ta=25°C, V_{CC}=20V unless otherwise specified.

Parameter	Terminal	Symbol	MIN	TYP	MAX	Unit
Operation Start Voltage	8 – 10	$V_{IN(ON)}$	15.8	17.6	19.4	V
Operation Stop Voltage	8 – 10	$V_{IN(OFF)}$	9.1	10.1	11.1	V
Circuit Current in Operation	8 – 10	$I_{IN(ON)}$	–	–	5	mA
Circuit Current in Non-operation	8 – 10	$I_{IN(OFF)}$	–	–	50	µA
Maximum OFF Time	–	$t_{OFF(MAX)}$	41	–	57	µs
Minimum Quasi-resonant Signal Input Time	9 – 10	$t_{th(2)}$	–	–	1.0	µs
Minimum OFF Time	–	$t_{OFF(MIN)}$	–	–	1.5	µs
OCP/FB Terminal Threshold Voltage 1	9 – 10	$V_{th(1)}$	0.70	0.76	0.82	V
OCP/FB Terminal Threshold Voltage 2	9 – 10	$V_{th(2)}$	1.3	1.5	1.7	V
OCP/FB Terminal Drawing Current	9 – 10	$I_{OCP/FB}$	1.0	1.35	1.5	mA
OVP Operation Power Supply Voltage	8 – 10	$V_{IN(OVP)}$	23.2	25.5	27.8	V
Latch Circuit Holding Current *3	8 – 10	$I_{IN(H)}$	–	–	70	µA
Latch Circuit Release Power Supply Voltage *3,4	8 – 10	$V_{IN(La.OFF)}$	7.9	–	10.5	V
Thermal Shutdown Operation Temperature	–	$T_{j(TSD)}$	135	–	–	°C

*3 Latch circuit is activated by overvoltage protection (OVP) and thermal shutdown (TSD).

*4 $V_{IN(OFF)} > V_{IN(La.OFF)}$

*5 Current characteristics are defined based on IC as Sink:+, Source:－.

6. Typical Application Circuit

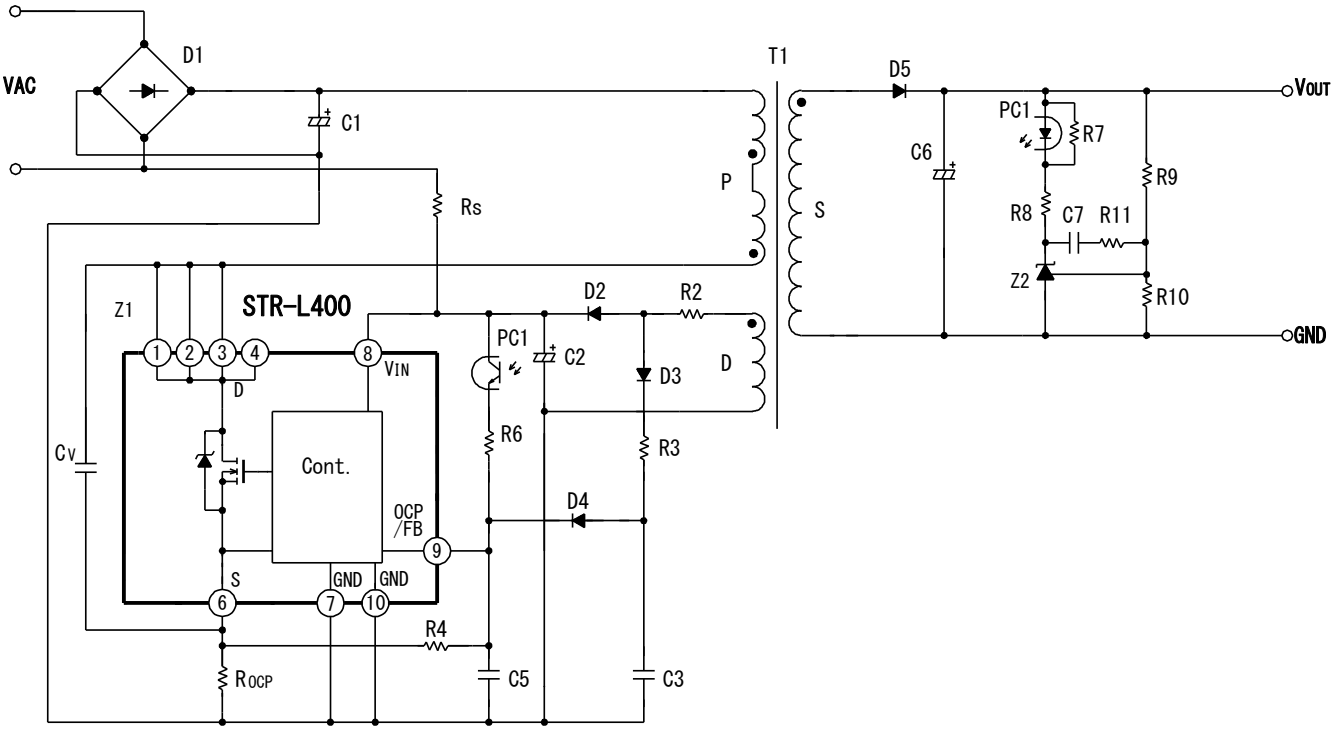


Fig.6 Typical application circuit

7. Functional Descriptions

7.1 Startup Operation

Fig.7-1 shows V_{IN} terminal peripheral circuit.

The startup circuit detects V_{IN} terminal voltage to effect the start/stop operation of the IC. At startup of the power supply, C2 is charged via a startup resistor R_S and when V_{CC} terminal voltage rises up to operation start power supply voltage $V_{IN\,(ON)}$ = 17.6V (TYP), the IC starts operation.

The R_S value is set so that the current of 100μA or higher flows in consideration of margin of the latch circuit holding current $I_{IN\,(H)}$ = 70μA (MAX). If the R_S value is too large, the charging time of C2 is prolonged after AC input and as a result, the startup time will be long. Therefore, it is also required to check the C2 capacitance.

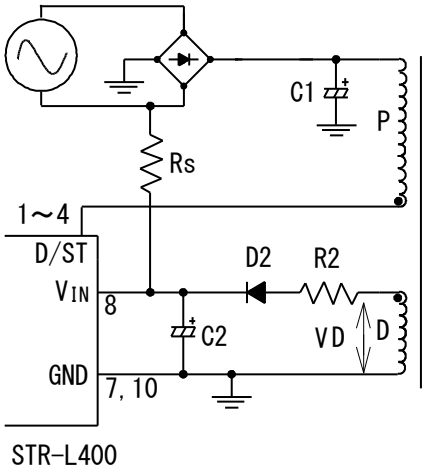


Fig. 7-1 V_{IN} terminal peripheral circuit

When the power supply specifications are standard ones, C2 is estimated to be 10 – 47μF , Rs to be 100 – 220kΩ at AC100V input and universal input, and to be 470 – 820kΩ at AC230V input.

Fig.7-2 shows the relation of V_{IN} terminal voltage and circuit current $I_{IN.}$ When V_{IN} terminal voltage reaches $V_{IN\,(ON)}$ = 17.6V(TYP), the control circuit starts operation and the circuit current increases. After the control circuit operation, when V_{IN} terminal voltage drops below the shutdown voltage $V_{IN(OFF)}$ = 10.1V(TYP), the control circuit stops operation by undervoltage lock out (UVLO) circuit and reverts to the state before startup. After the control circuit operation, the voltage that is rectified from auxiliary winding D in Fig.7-1 becomes the power source to V_{IN} terminal. The auxiliary winding voltage needs to be adjusted to approximately 18V, taking into account the turn's ratio of auxiliary winding D, so that V_{IN} terminal voltage becomes:

$$V_{IN(OFF)} = 11.1V(MAX) < V_{IN} < V_{IN(OVP)} = 23.2V(MIN)$$

within the limits for input and output deviation.

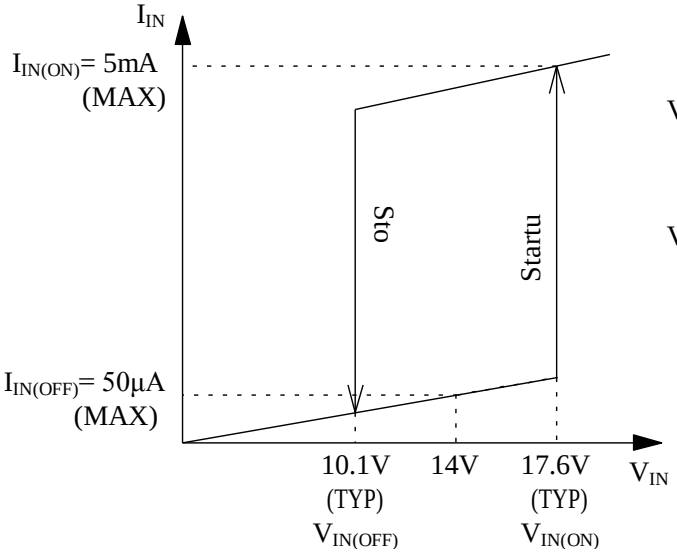


Fig.7-2 V_{IN} Terminal Voltage - Circuit Current I_{IN}

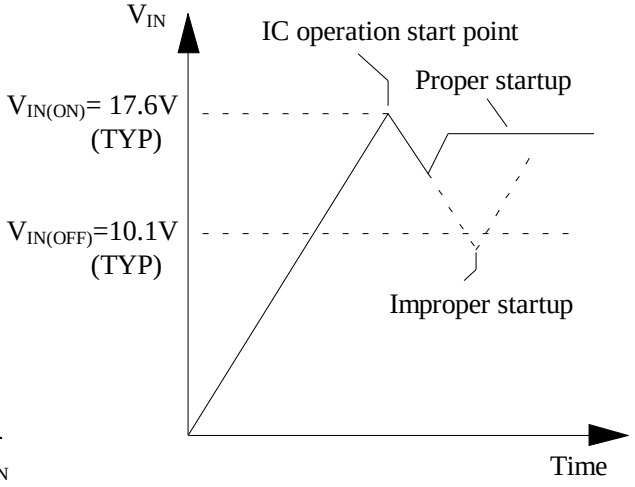


Fig.7-3 V_{IN} terminal voltage waveform at startup

An example of the waveform of V_{IN} terminal voltage is shown in Fig. 7-3.

When the V_{IN} terminal voltage reaches $V_{IN\ (OFF)}$ to result in startup failure as shown in Fig.7-3, the capacitance of C2 should be increased. As the capacitance is increased, the startup time is prolonged. Therefore, it should be checked whether the long startup time does not give any trouble to the operation or not.

In actual power supply circuits, there are cases in which V_{IN} voltage fluctuates in proportion to the secondary output current $I_{OUT,}$ (see Fig.7-4) to effect overvoltage protection (OVP). This happens because C2 is charged to a peak by the transient surge voltage that is generated at the moment power MOSFET turns off. To prevent this, it is effective to add some value R2, of several ohms to several tenths of an ohm, in series with rectification diode D2 (see Fig.7-5). The optimal value of R2 shall be determined using a transformer matching the application, because the proportion of V_{IN} voltage versus the transformer output voltage differs according to transformer structural design. The proportion of change between V_{IN} voltage versus the transformer output voltage becomes worse if:

- The coupling between the primary winding and the secondary winding of transformer get worse(low output voltage, large current load specifications etc.).
- The coupling between the auxiliary winding D and the stabilizing output winding (a winding of the circuit that controls a constant voltage) gets worse.

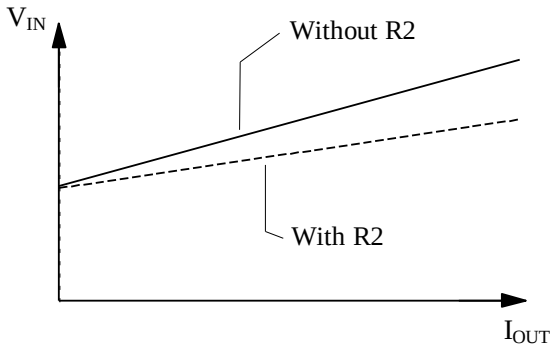


Fig. 7-4 Output current I_{OUT} by R2 - V_{IN} Terminal Voltage

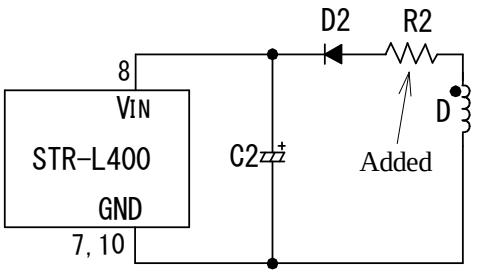


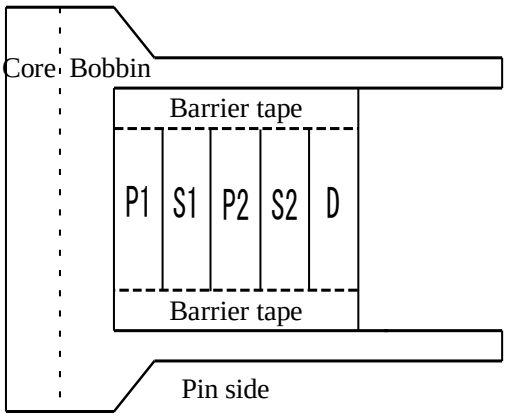
Fig. 7-5 V_{IN} terminal peripheral circuit that is insusceptible to output current I_{OUT}

For transformer design, Fig.7-6 and 7-7 show reference examples of the position of auxiliary winding D.

- Separate the auxiliary winding D from the primary winding P1 and P2 with wider distance (Fig. 7-6 winding structure example 1).

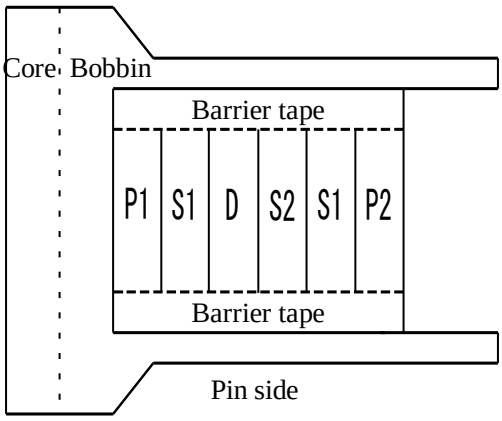
  The primary winding is divided into two as P1 and P2 (sandwiched windings)
- Sandwich the auxiliary winding D with the secondary stabilizing output winding S1 (Fig. 7-7 winding structure example 2).

  Only S1 is a stabilized output winding (output line winding controlled to constant current) out of two output winding S1 and S2.



P1, P2: Primary winding
S1: Secondary control winding
S2: Secondary output winding
D: Auxiliary winding for V_{CC}

Fig. 7-6 Winding Structure 1



P1, P2: Primary winding
S1: Secondary control winding
S2: Secondary output winding
D: Auxiliary winding for V_{CC}

Fig. 7-7 Winding Structure 2

7.2 Constant Voltage Control Circuit Operation

The output voltage is controlled to constant voltage by the current mode control (peak current mode control) that has superior transient responsibility and stability. Fig. 7-8 shows a FB/OLP terminal peripheral circuit and Fig. 7-9 shows a constant voltage control.

The feedback current according to a load generates the voltage drop VR4 in R4 through a photo coupler PC1.

The constant voltage control is done in the current control mode where OCP/FB terminal voltage which superimposes VR4 on voltage fall VR_{OCP} generated at a detection resistor by drain current, is compared with OCP/FB terminal threshold voltage $1V_{th\,(1)}$ = 0.76V (TYP) by an OCP comparator (OCP Comp) in the IC.

In the current mode control, the voltage of VR4 rises at light load and the OCP comparator (OCP Comp) malfunctions due to the steep surge current generated at turn-on of the power MOSFET, resulting in turning - off of the power MOSFET.

In order to prevent this malfunction, the STR-L400 series incorporates an active low pass filter circuit. Until the power MOSFET turns on, the OCP /FB terminal is drawn at the constant current of OCP/FB terminal drawing current $I_{OCP/FB}$ = 1.35 mA to decrease the bias amount by half. The surge voltage generated at turn-on of the power MOSFET is absorbed by C5 by using this circuit to assure stable operation up to light load.

Typical constants of R4, R6 and C5 are estimated to be R4 =680Ω, R6 = 3.3kΩ and C5 = 100p – 470 pF respectively. When C5 capacitance is too large, the response of OCP is delayed, therefore it should be noted that the drain current peak may be increased at the transient state such as power supply startup. When malfunction occurs, the constants should be checked in reference to the actual operation.

The operation mode of STR-L400 series is switched to either one of the following two modes according to the state whether quasi resonant signal is present or not.

- PRC (Pulse Ratio Control) operation
- Quasi resonant operation

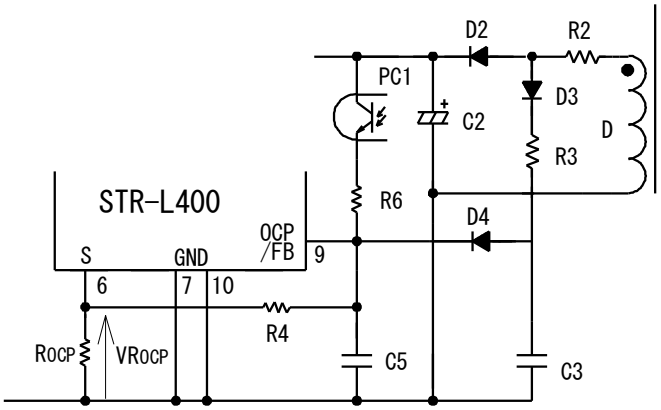


Fig. 7-8 OCP/FB terminal peripheral circuit

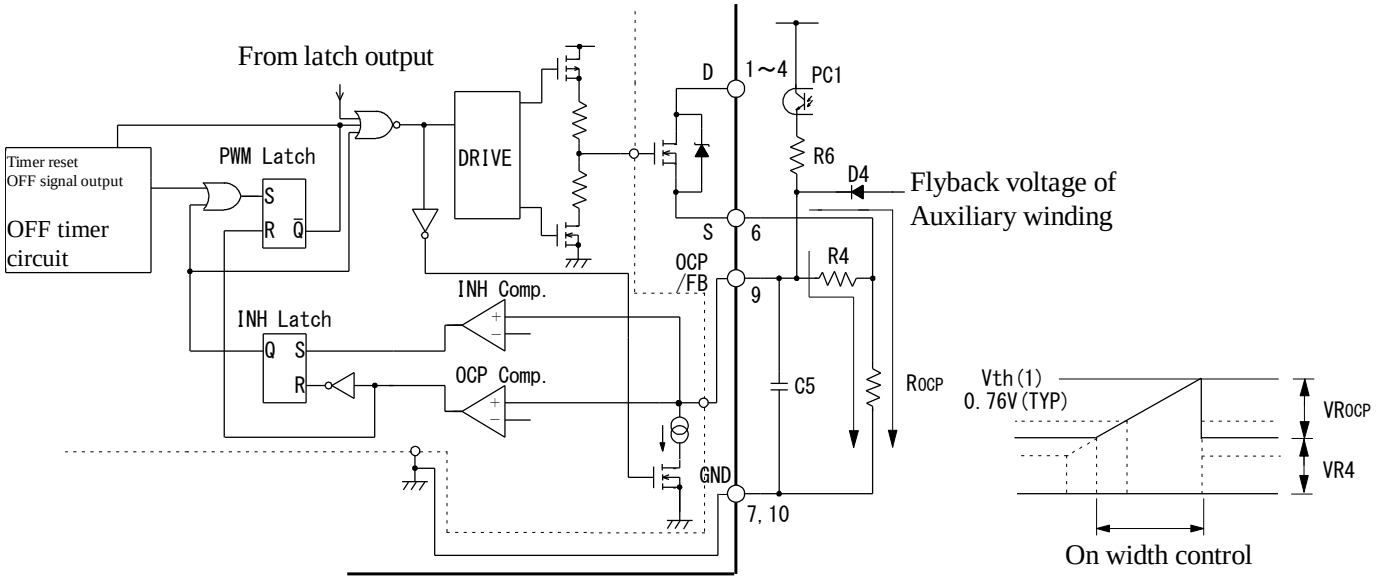


Fig. 7-9 Constant voltage control operation

7.2.1 PRC Operation

If there exists no quasi resonant signal or it is not yet established (OCP/FB terminal voltage $2V_{th\,(2)}$ = 1.5V (TYP) or lower), operation is performed by the maximum OFF time $t_{OFF\,(MAX)}$ = 50μs (TYP) fixed, ON time control.

In the case that the power MOSFET turns on, after the OFF time internally fixed by the OFF timer circuit in Fig. 7-9, the Q of Latch is latched to L and the power MOSFET turns on when the gate drive conditions are met.

In the case that the power MOSFET turns off, the OCP/FB terminal voltage exceeds the OCP/FB threshold voltage $1V_{th\,(1)}$ = 0.76V (TYP) by the OCP comparator (OCP Comp) and the Q of Latch is latched to H to turn off the drive circuit and turn off the power MOSFET.

Since OFF time is 50μs (TYP) fixed, the switching frequency at PRC operation is about 20kHz to decrease the stress of components at startup or output short circuit, when quasi resonant signal is not yet established.

The power consumption at such minimal load as standby load can be decreased by adding a circuit which cuts the quasi resonant signal by external signals.

7.2.2 Quasi Resonant Operation

When OCP/FB terminal voltage exceeds $V_{th(2)}$ = 1.5V (TYP) due to the quasi resonant signal generated by the

auxiliary winding, the OFF timer circuit in the IC is switched to the minimum OFF time $t_{OFF\,(MIN)}$ = 1.5μs (MAX) and the power MOSFET continues to be off until the OCP/FB terminal voltage becomes $V_{th\,(1)}$ = 0.76V (TYP) or lower. The quasi resonant operation is performed by this operation. Refer to 7.3 Bottom timing (quasi resonant signal) for quasi resonant operation.

7.3 Bottom-ON Timing (Quasi-resonant Signal)

As shown in Fig. 7-10, the flyback system (which provides energy to the secondary side, when the power MOSFET is OFF) performs free vibration at a frequency where the drain voltage V_{DS} is determined by the capacitor Cv between the transformer L_P and the drain source after releasing energy to the secondary side.

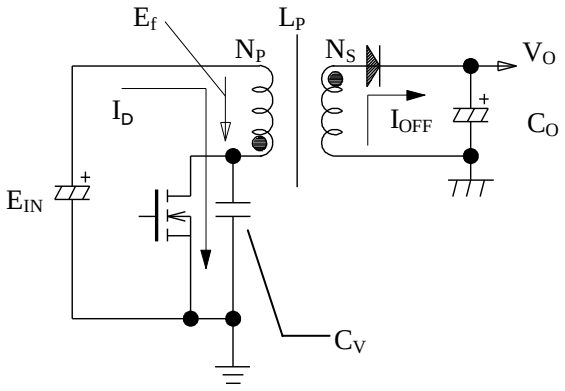


Fig. 7-10 Flyback system

E_{IN}: DC voltage

Ef: Flyback voltage $Ef = \frac{Np}{Ns} \times (Vo + V_F)$

N_P: Primary winding

N_S: Secondary winding

V_O: Output voltage

V_F: Forward voltage drop of diode

I_D: Drain current of power MOSFET

I_{OFF}: Current flowing across secondary diode when power MOSFET is OFF.

C_V: Voltage resonant capacitor

L_P: Excitation inductance

Turning- ON of the power MOSFET at the bottom point of free vibration of V_{DS} is called bottom-ON and Fig. 7-11 shows the V_{DS} waveform at ideal bottom-ON.

In the quasi resonant operation, turning-ON is performed at V_{DS} bottom point to reduce switching loss and switching noise, resulting in the realization of high efficiency and low noise.

The delay timing which turns the power MOSFET on during the period of free vibration of V_{DS} is made from the auxiliary winding voltage synchronized with V_{DS} waveform.

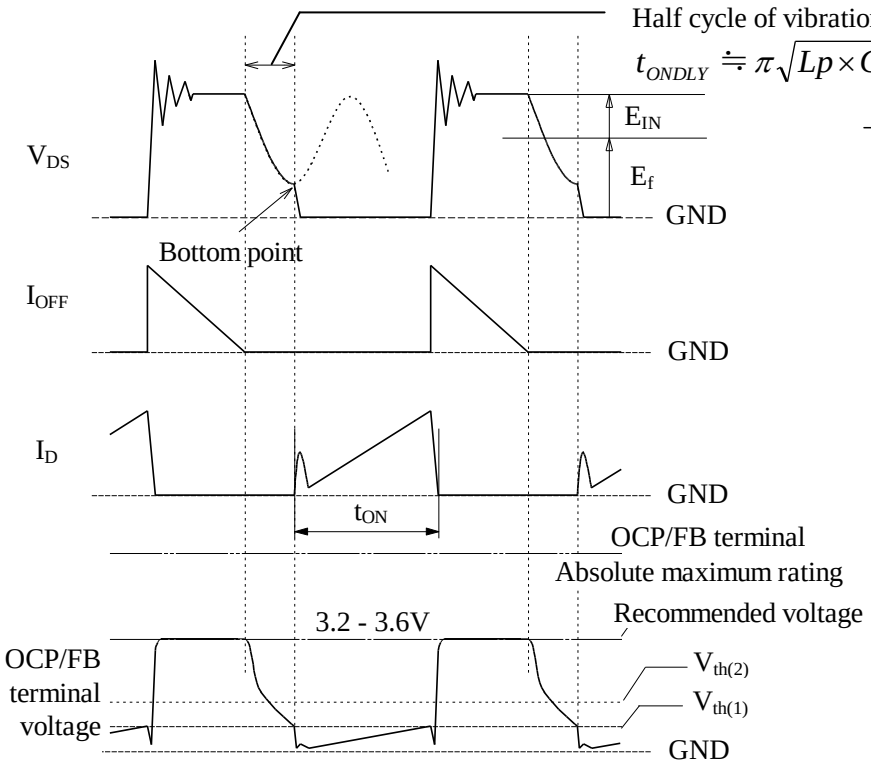


Fig. 7-11 Ideal bottom-on: the turn-on timing is at the bottom point of V_{DS} waveform

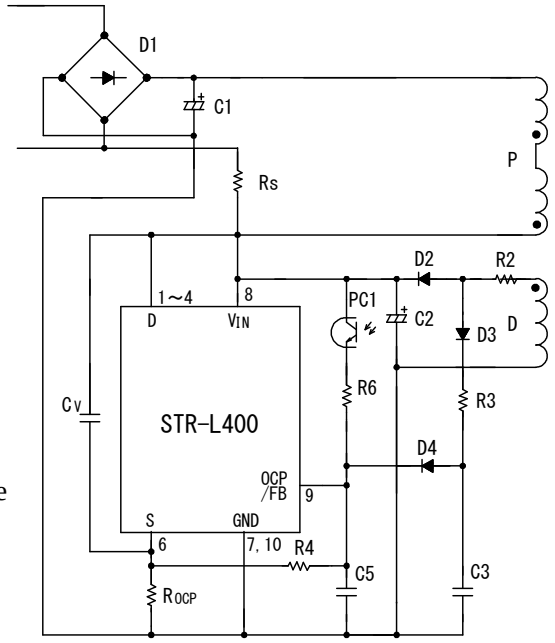


Fig. 7-12 Quasi-resonance and delay circuit

D3, D4, R3 and C3 between the auxiliary winding D and OCP/FB terminal shown in Fig. 7-12 compose the delay circuit.

After turn-off of the power MOSFET, when OCP/FB terminal voltage is increased to OCP/FB threshold voltage 2 $V_{th\,(2)}$ = 1.5V (TYP) or higher by the auxiliary winding voltage, the INH comparator in the IC is operated to continue the OFF state of power MOSFET until it falls to the OCP/FB terminal threshold voltage 1 $V_{th\,(1)}$ = 0.76V (TYP).

When the energy of the transformer has been discharged, the auxiliary winding voltage begins to fall. C3 and C5 voltages are discharged by the synthesized impedance of the active low pass filter circuit and R4 in the IC and when the OCP/FB terminal voltage falls below $V_{th\,(1)}$, the power MOSFET turns on.

The discharging period is equivalent to the delay time. C3 is adjusted by observing the operation waveform in a manner that the delay time becomes bottom-ON. The malfunction of quasi resonant operation is prevented by the voltage difference between $V_{th\,(1)}$ and $V_{th\,(2)}$ and the active low pass filter circuit.

Quasi resonant signal voltage of OCP/FB terminal:

- In the case that it is too low:

The startup failure occurs if the switching from PRC operation to quasi resonant operation is delayed, the rise of the output voltage is delayed and the V_{IN} terminal voltage falls to the operating power supply stop voltage.

- In the case that it is too high:

The power MOSFET may turn ON/OFF at high frequency due to malfunction at startup of power supply. If the

channel temperature exceeds the maximum rating, the MOSFET is damaged.

- In the case that it includes large ringing waveforms:

Fig. 7-13 shows the BD terminal waveform using a transformer with poor coupling.

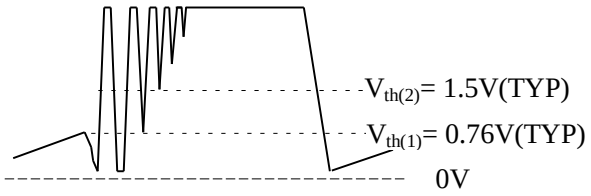


Fig.7-13 BD terminal waveform using a poor coupling transformer

If the turn ratio of primary winding and secondary control winding (N_P/N_S) is extremely large (in the low voltage and high current load specifications), a surge voltage may be generated on BD terminal voltage thought auxiliary winding in MOSFET turning off, and the power MOSFET may be switched with high frequency by the detection of ringing voltage as a quasi-resonant signal.

When high frequency operation occurs, such adjustments as connection of R4, R5 close to of OCP/FB terminal - GND terminal, separation of OCP/FB terminal - GND pattern loop from high current pattern, use of winding method for lessening coupling force of primary and secondary windings or adjustment of constants of clamp snubber should be made to avoid high frequency operation.

In addition, the probe which confirms the operation waveform of the OCP/FB terminal should be connected close to OCP/FB terminal and GND terminal.

The quasi resonant signal of OCP/FB terminal is adjusted as follows:

- Selection of delay circuit

It is selected from 7.4 Types of delay circuit" according to power supply specifications.

The following adjustments will be explained with a circuit example B (basic circuit with the most wide application range) of 7.4 Types of delay circuits.

- Amplitude of quasi resonant signal and effective period

Recommended waveforms are shown in Fig. 7-14.

The current I_S flowing across R3 at quasi resonant operation is as shown in the following formula (1) since the constant current 1.35mA of R4 and active low pass filter circuit is connected if the recommended value is 3.4V. R_{OCP} is not considered in the calculation formula since it is much smaller than R4 and negligible.

$$Is = \frac{3.4V}{R4} + 1.35mA$$

$$R3 = \frac{V_D - 3.4V - 2 \times V_F}{I_S} \qquad (1)$$

In this formula, V_D is auxiliary winding voltage and V_F is forward voltage drop of D3 and D4 ≈ 0. 7V.

R3 should be determined in consideration of the following for the adjustment of quasi resonant signal.

Amplitude should be adjusted to be 3.2 - 3. 6V at AC input voltage MIN, Po = MAX. OCP/FB terminal voltage requires the setting of the absolute maximum rating of 6V or lower.

The effective period requires time of 1μs or longer so as to assure Vth (2) = 1.7V at the AC input voltage MIN, Po = MIN. If the period is short, the quasi resonant operation may be unable to follow up in the case of the power supply specifications of higher switching frequency. When the effective period cannot be adjusted, it is required to review the circuit type D in 7.4 Types of delay circuits or to consider the increase of inductance of transformers for lowering the switching frequency.

It should be confirmed that there is no malfunction due to noise and that operation is performed with the OFF time of about 50μs during the PRC operation period at power supply startup (The OFF time gets shorter if the noise enters the OCP/FB terminal).

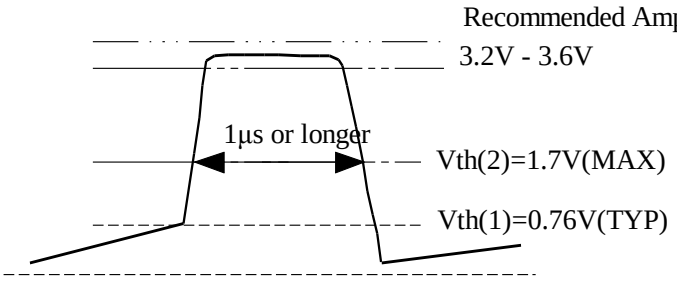


Fig. 7-14 OCP/FB terminal voltage waveform

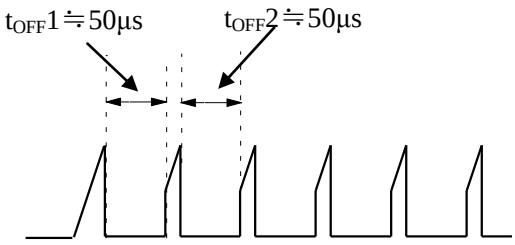


Fig. 7-15 Drain current waveform in power supply startup

In order to adjust the bottom point of V_{DS}, actual waveforms of V_{DS}, $V_{OCP/FB}$ (OCP/FB terminal voltage waveform) and I_D should be observed to adjust the delay time t_{ONDLY} in a manner that the ideal bottom-ON in Fig. 7-16 (turning ON at bottom of V_{DS}) is achieved.

When turn-ON is earlier than the bottom point (Fig. 7-17) on the condition that AC input voltage and Po are maximum, the capacitance of C3 initially connected should be increased and after confirming the bottom point, it should be adjusted so that the turn-ON is made in conformity with the bottom point of V_{DS}.

When turn-ON is later than the bottom point (Fig. 7-18) on the condition that AC input voltage and Po are maximum, the capacitance of C3 initially connected should be decreased and after confirming the bottom point, it should be adjusted so that the turn-ON is made in conformity with the bottom point of V_{DS}.

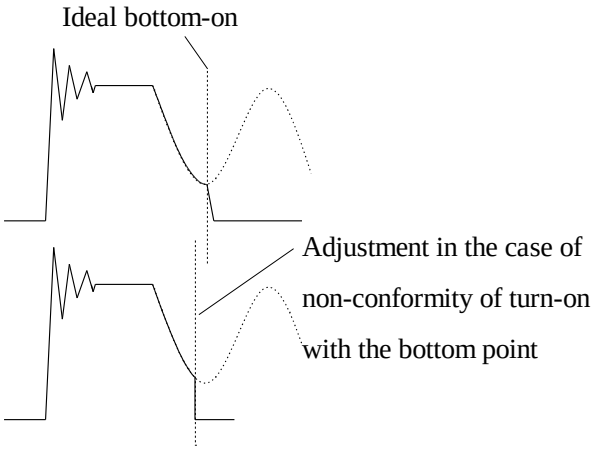


Fig. 7-16 Bottom-ON setting

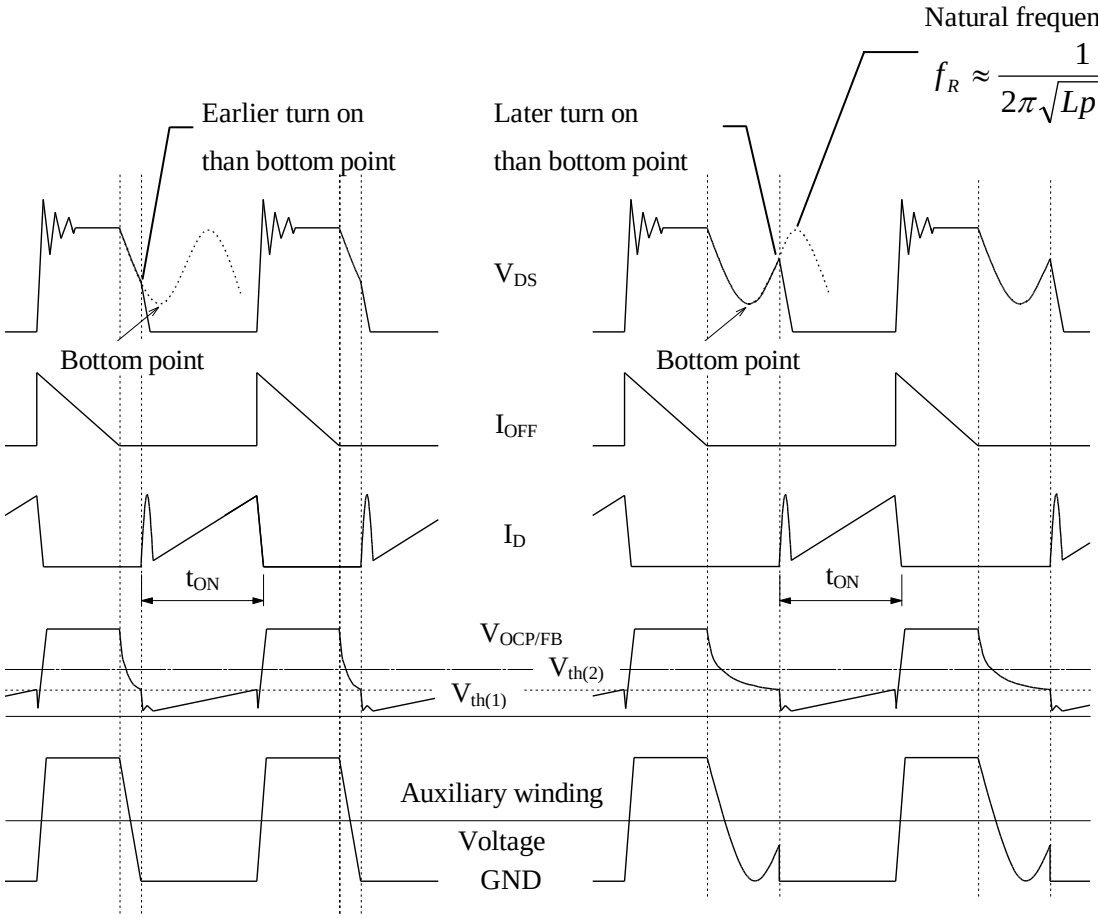


Fig. 7-17 Example of earlier turn on than bottom point of V_{DS}

Fig. 7-18 Example of later turn on than bottom point of V_{DS}

In the case that turn-on is not in conformity with the bottom point of V_{DS} at adjustment, it should be set prior to the bottom point as stipulated in Fig. 7-16 (Adjustment in the case of non-conformity of turn-on with the bottom point). When it is set after the bottom point, oscillation may be unstable.

7.4 Types of Delay Circuit

The delay circuit structure is shown in Fig. 7-19.

- Type A circuit:

This is a circuit with few components and the highest attenuation effect of surge voltage. However, since the loss of R3 becomes large, the capacitance of C3 cannot be increased. Therefore, this circuit is not suitable for a power supply with high natural frequency or a narrow input power supply.

- Type B circuit

Longer time can be set compared to type A. This type is the most widely applicable and typical circuit with the high attenuation effect of surge voltage.

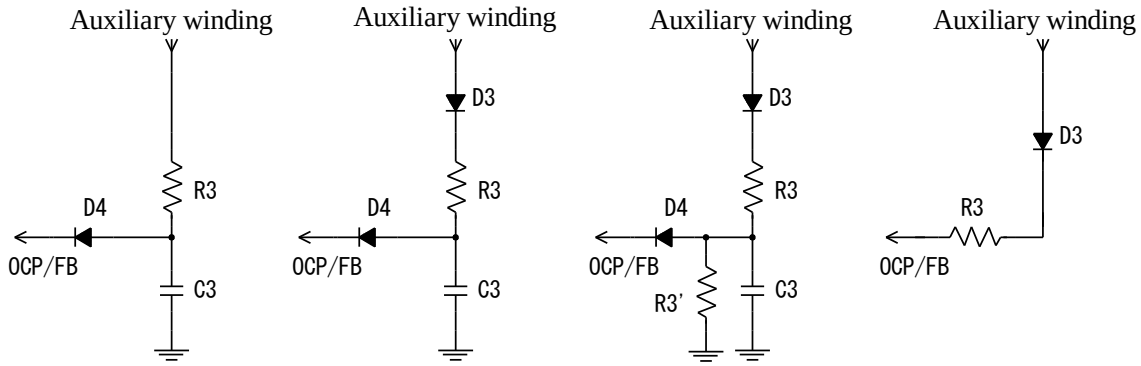
- Type C circuit

As the electric charges of C3 are discharged by R3', change in delay time due to feedback current is small in this circuit. This type of circuit is suitable in the case of sudden change of load or for the universal input power supply requiring the wide adjustment range of delay time. It is necessary to compensate the value of R3 since the current

flowing across R3 by R3' is bypassed.

- Type D circuit

This type of circuit has the lowest part count and can follow up to the switching frequency of about 300kHz. However, the delay time cannot be adjusted. This type of circuit is suitable in the case that 1/2 of natural frequency conforms to the delay time ($\pi\sqrt{L_P \times C_V} \approx$ 1.5μs or so), or slight increase of switching loss does not create any problem although the turn-on timing of the power MOSFET is not in conformity. This circuit is also appropriate for AC100V series power supply with small output power or a universal input power supply with high natural frequency and small output power.



Type A circuit Type B circuit Type C circuit Type D circuit

Fig. 7-19 Types of delay circuit

7.5 Latch Cirtcuit

The latch circuit stops switching operation (latch off) in each operation of overcurrent protection (OVP) and thermal shutdown (TSD) circuit.

When the latch circuit is operated and the switching operation is stopped, the V_{IN} terminal voltage begins to fall and when the V_{IN} terminal voltage falls to $V_{IN\ (OFF)}$ =10.1V (TYP), the circuit current becomes 50μA or less and the V_{IN} terminal voltage commences to rise. Then, when it reaches the operation start power supply voltage $V_{IN\ (ON)}$ =17.6V (TYP), the circuit current is increased and the V_{IN} terminal voltages falls. V_{IN} terminal voltage waveform at latch circuit operation rises and falls between 10.1V (TYP) and 17.6V (TYP) as shown in Fig. 7-20 to prevent the abnormal rise of the V_{IN} terminal voltage. Though the latch circuit holding current $I_{IN\ (H)}$ is 70μA (MAX) at V_{IN} = 9.8V (TYP), a startup resistor R_S which can flow 100μA or higher should be set with margin considered.

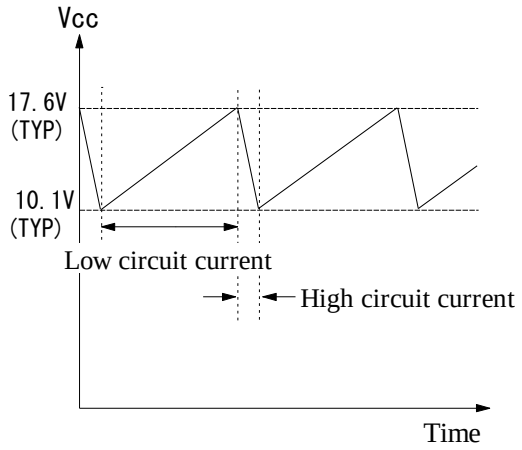


Fig. 7-20 V_{IN} terminal voltage waveform in latch

The latch circuit is released by shutting-down the AC input and reducing V_{IN} terminal voltage to $V_{IN(La.OFF)}$= 7.9V(MIN) or lower.

7.6 Overvoltage Protection (OVP)

When the voltage of OVP operation power voltage $V_{IN(OVP)}$= 25.5V(TYP) or higher is applied between V_{IN}

terminal and GND terminal, the overvoltage protection function operates and the switching operation stops in latch mode.

If V_{IN} terminal voltage is supplied from the auxiliary winding of transformer, the secondary overvoltage can be detected, in output voltage detection circuit open or others, because V_{IN} terminal voltage is proportional to output voltage.

In this case, the secondary output voltage in the operation of overvoltage protection is calculated according to the following formula (2).

$$V^{OUT(OVP)} = \frac{\text{Output voltage in normal operation}}{V_{IN}\text{ terminal voltage in normal operation}} \times 25.5\text{V(TYP)} \quad \text{---} \quad (2)$$

7.7 Thermal Shutdown (TSD)

The switching operation is stopped in latch mode when the temperature of IC control circuit reaches the thermal protection operation temperature $T_{j(STD)}$=135°C (MIN) or higher.

7.8 Overcurrent Protection (OCP)

The overcurrent protection circuit (OCP) detects the peak power MOSFET drain current by pulse-by-pulse method and limits the power.

The power MOSFET drain current is detected by the current detection resistor R_{OCP} between OCP/FB terminal and GND terminal, and the power MOSFET turns off when the voltage drop of R_{OCP} reaches the OCP/FB terminal threshold voltage $1V_{th(1)}$= 0.76V(TYP).

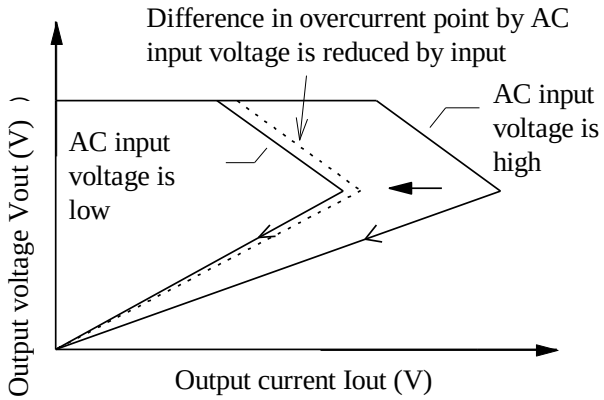


Fig. 7-21 Output over load characteristics

When the output voltage falls in the overload state, the auxiliary winding voltage also falls proportionally. When V_{IN} terminal voltage falls below the operation stop voltage $V_{IN\ (OFF),}$ the switching operation is stopped and the circuit current is decreased and as a result, V_{IN} terminal voltage commences to rise. When it reaches the operation start power supply voltage $V_{IN\ (ON)}$ = 17.6V (TYP), the control circuit is again operated to perform intermittent operation by UVLO.

Since the coupling of transformer of multi output windings is poor, the auxiliary winding voltage may not fall and intermittent operation may not be performed even if the output voltage falls in the overload state. In this case, it is required to review the construction of the transformer for enhancing the coupling between the secondary side winding and the auxiliary winding.

7.8.1 Overcurrent Input Compensation

For the compensation of overcurrent by AC input voltage, the overcurrent in high input voltage is operated at earlier timing by R_A, R_B and D_Z in Fig. 7-22 and the difference from the low input voltage can be reduced as shown in Fig. 7-21.

For the compensation of overcurrent input, the surge voltage generated from the transformer is reduced to suppress the drain current peak of power MOSFET to a low level and the stress of the secondary side rectifier diode and the power MOSFET at startup of power supply and overload can be decreased.

$$R_A = 680\Omega \times \frac{E_{IN(MAX)} - E_{IN(MIN)}}{0.76V} \times \frac{I_{DP(MAX)}}{I_{DP(MAX)} - I_{DP(MIN)}}$$

$$R_B = \frac{(6.8V + 0.76V)}{E_{IN(MIN)} - (6.8V + 0.76V)}$$

$I_{DP(MAX)}$: $V_{IN\ (AC)\ (MIN)}$, Po = drain current at MAX

$I_{DP(MIN)}$: $V_{IN(AC)(MAX)}$, Po=drain current at MAX

$E_{IN(MIN)}$:C1 voltage at $V_{IN\ (AC)\ (MIN)}$

$E_{IN(MAX)}$:C1 voltage at $V_{IN\ (AC)\ (MAX)}$

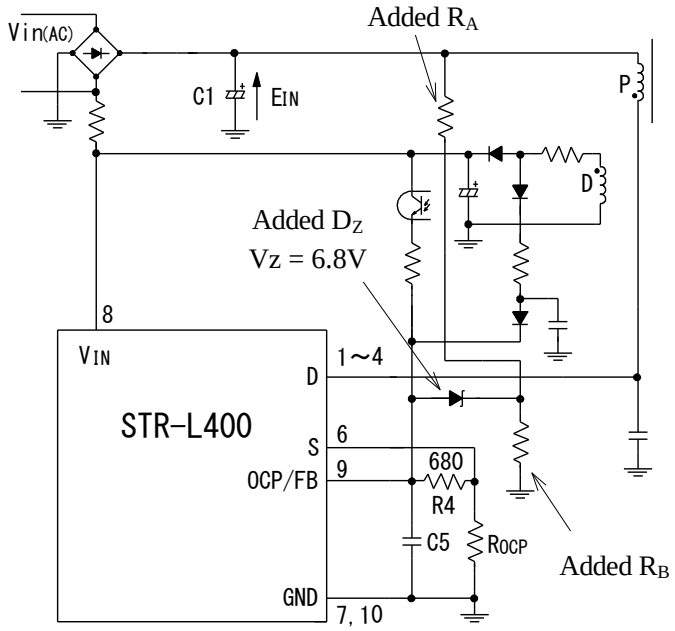


Fig. 7-22 Overcurrent input compensation circuit

8. Design Notes

8.1 External Components

Take care to use properly rated, including derating as necessary and proper type of components.

- Input and output electrolytic capacitors. Apply proper derating against ripple current, voltage, and temperature rise. Use of high ripple current and low impedance types, designed for switch mode power supplies, is recommended.
- Transformer. Apply proper derating against core temperature rise from core loss and copper loss.
- A high frequency switching current flows to Current sensing resistor R1 ($_{ROCP}$), and may cause poor operation if a high inductance resistor is used. Choose a low inductance and surge-proof type.

8.2 Control of Switching Speed

As the source terminal (pin 6) of STR-L400 series is independent, it is possible to reduce the switching noise by inserting a ferrite bead FB into this pin and adjusting the switching speed.

When the ferrite bead FB is inserted, the switching speed is dropped not only at the turn-on of the power MOSFET, but also at the turn-off thereof, possibly resulting in the increase of switching loss.

Therefore, the drop in switching speed at turn-off can be prevented by inserting the diode D6 shown in Fig. 8-1. For a diode to be inserted, either a small-signal switching diode with small junction capacitance at high speed or a Schottky barrier diode (Sanken's AK03 etc.) should be used.

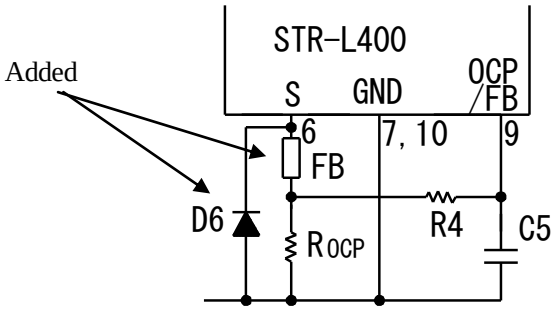


Fig. 8-1 Circuit example of insertion between source terminal and GND terminal

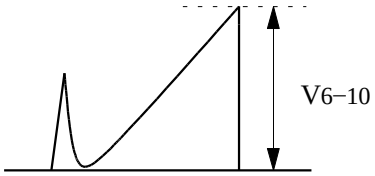


Fig. 8-2 Voltage curve between pin 6 and pin 10.

When the ferrite bead FB for speed control is inserted, the voltage fall will occur for this insertion. The voltage fall between the source terminal (pin 6) and the ground terminal (pin 10) is increased and the V_{GS} voltage between gate and source of the power MOSFET falls and the drive voltage also falls.

Since the maximum switching current* of power MOSFET is reduced, the voltage between the source terminal and the ground terminal should be measured and the maximum switching current should be derated from the maximum switching current derating curve described in the product specifications.

It should be confirmed that the voltage fall between the source terminal (pin 6) and the ground terminal (pin 10) and the maximum switching current are within the maximum switching current derating curve in normal operation and overcurrent protection operation.

* The maximum switching current:

This is drain current is determined by the drive voltage in the IC and T_{th} of power MOSFET. When the voltage fall between the source terminal (pin 6) and the ground terminal (pin 10) occurs due to pattern drawing etc., the maximum switching current is decreased by the V_{6-10} in Fig. 8-2. Therefore, it should be used within the maximum switching current derating curve described in the product specifications.

8.3 Transformer Design

The designing of transformers is basically the same as the power supply transformers of RCC method (Ringing Choke Converter: self-exciting type flyback converter).

However, as the duty is varied to the extent that the turn-on is delayed by the quasi resonant operation, the compensation of the duty is required.

When the ON Duty obtained by the ratio of the primary winding N_P and the secondary winding Ns is expressed as D_{ON}, Lp is obtained from the following formula (3).

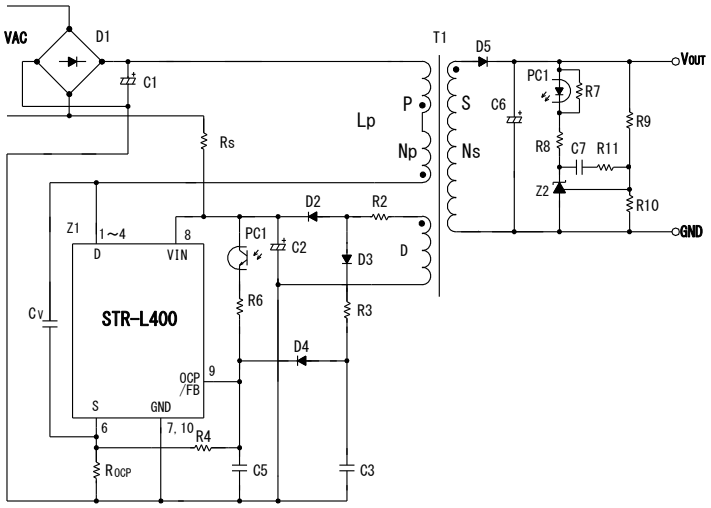


Fig. 8-3 Circuit example

$$L_P = \frac{\left(Ein(MIN)\cdot D_{ON}\right)^2}{\left(\sqrt{\frac{2\cdot P_O\cdot f_O}{\eta_1}} + Ein(MIN)\cdot\pi\cdot f_O\cdot D_{ON}\cdot\sqrt{Cv}\right)^2} \quad (3)$$

L_P is calculated under the following conditions:

Po: Maximum output power

fo: Minimum oscillating frequency

η1: Conversion efficiency of transformer

D_{ON}: ON Duty at Vin (AC) MIN⇒ $D_{ON} = \frac{Ef}{E_{in(MIN)} + Ef}$

Ein (MIN): Voltage between C1's at Vin (AC) MIN

Ef: Flyback voltage ⇒ $Ef = \frac{Np}{Ns}\times\left(Vout + V_F\right)$

V_F: Forward voltage drop of D5

Each parameter such as drain current peak I I_{DP} is calculated from the following formula.

$$t_{ONDLY} = \pi\sqrt{L_P\times Cv} \quad (4)$$

$$Don' = \left(1 - f_O\times t_{ONDLY}\right)\times Don \quad (5)$$

$$Iin = \frac{P_O}{\eta_2}\times\frac{1}{Ein(MIN)} \quad (6)$$

$$I_{DP} = \frac{2\times Iin}{Don'} \quad (7)$$

$$Np = \sqrt{\frac{L_P}{AL-Value}} \quad (8)$$

$$Ns = \frac{Np \times (Vout + V_F)}{Ef} \quad (9)$$

t_{ONDLY}: Delay time

Iin: Average input current

η_2: Conversion efficiency of power supply

I_{DP}: Switching current peak

Don´: ON Duty after compensation

With respect to the AL-Value of transformer ferrite core, the AL-Value which never causes magnetic saturation should be selected in consideration of NI-Limit (AT) value that is calculated from N_P and I_{DP}. The calculated NI-Limit value (= I_{DP} x Np) is required to be always within the area of the NI-Limit vs. AL-Value characteristic curve (shaded area) in the Fig.8-3. When the ferrite core which meets the relation of the NI-limit vs. AL-Value is selected, it is recommended to set the calculated NI-Limit value in a manner that it is around 30% lower than the NI-Limit in the core data in consideration of design margin to the variation of temperature etc.

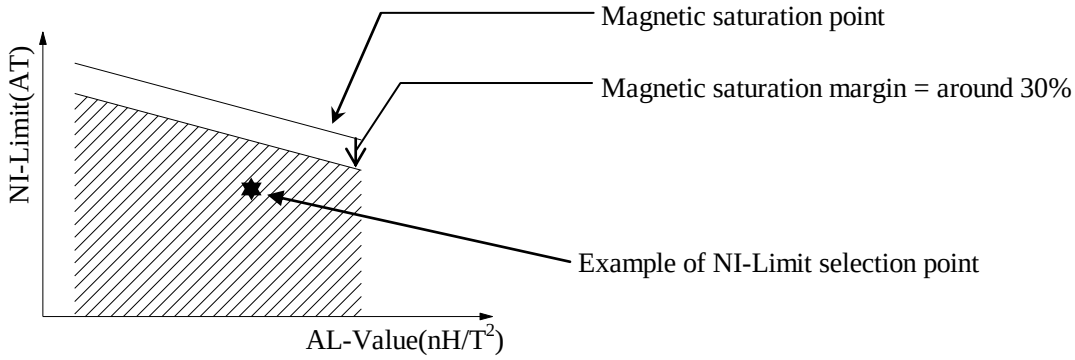


Fig. 8-3 NI-Limit vs. AL-Value Characteristics of Core

Therefore, the NI-Limit is set to the value in consideration of saturation margin from the following formula.

$$NI = Np \times I_{DP}(130\%) \quad (10)$$

The minimum oscillation frequency fo is calculated from the ON Duty after compensation by the following formula.

$$f_O = \left(\frac{-\sqrt{\frac{2P_O}{\eta_1}} + \sqrt{\frac{2P_O}{\eta_1} + \frac{4 \times \pi \times (Ein(MIN) \times Don)^2 \times \sqrt{Cv}}{\sqrt{Lp}}}}{2 \times Ein(MIN) \times \pi \times Don \times \sqrt{Cv}} \right)^2 \quad (11)$$

Points to be considered in designing the transformer winding

The high-frequency element is included in switching current, and the skin effect may affect. Therefore, the winding wire diameter used for transformer shall be selected so that the current density is in the range of 3 to 4A/mm^2, considering the root mean square value of operating current. When the additional measures against temperature are needed due to the skin effect or others, the following should be examined in order to increase the winding wire surface area.

- Increase the number of winding wire
- Use the litz wire
- Enlarge the wire diameter

8.4 Phase Compensation

Fig.8-4 shows the circuit diagram for the secondary error amplifier, using a general shunt regulator. As for the phase compensation capacitor, C7, the capacitance shall be adjusted in the range of 0.047 - 0.47μF, and finally determined on actual operations.

In normal operation, no additional component is required for phase compensation. However, only the compensation of the secondary side may not be sufficient when the output load specification is a dynamic load with large amplitude or the ripple current of secondary side smoothing capacitor is large. When the compensation of the secondary side is not sufficient, C8 and D6 should be added as shown in Fig. 8-5 to assure the stability.

C8 is estimated to 0.01μF - 0.1μF and when the C8 is added, D6 which prevents the current from flowing in the reverse direction should be added.

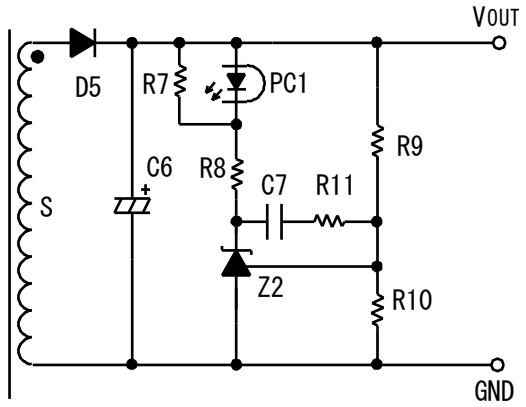


Fig.8-4 Peripheral circuit around shunt regulator (Z2)

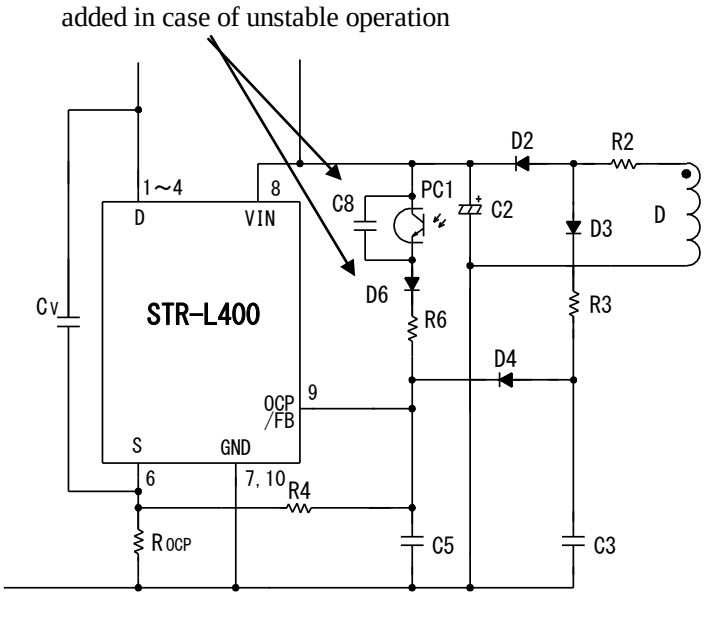


Fig.8-5 OCP/FB terminal peripheral circuit

8.5 Component Layout and Trace Design

PCB circuit trace design and component layout affect proper functioning during malfunctions, EMI noise, and power dissipation.

Therefore, where high frequency current traces form a loop, as in Fig.8-6, the design with the wide, short patterns, small circuit loops and the low line impedance is required. In addition, local GND and earth ground traces affect radiated EMI noise, thus the same measures should be taken into account.

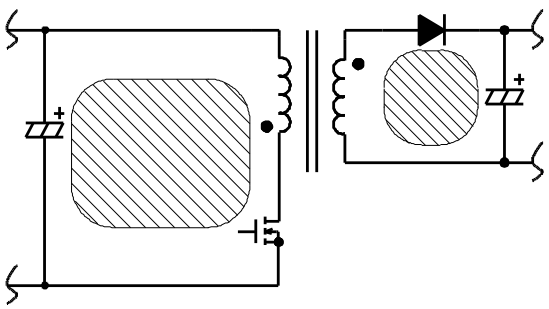


Fig.8-6 High frequency current loops (hatched areas)

Switching mode power supplies consist of current traces of high frequency and high voltage, thus trace design and component layouts should be done to comply with all safety guidelines.
Furthermore, in the case where a power MOSFET is being used as the switching device, take into account the positive thermal coefficient of $R_{DS(on)}$ when preparing a thermal design.

Fig. 8-7 shows the example of peripheral circuit connection.
(1) Around source terminal (S) (S terminal - R_{OCP} - C1 - T1(P winding) - D terminal)
This is the main circuit containing the switching current, and thus it should be as wide and as short as possible. In case the distance between C1 and the device is lengthy, an isolation capacitor near the device or the transformer is recommended.
The capacitors may be either electrolytic or film type capacitors, 0.1μF, in the range considered maximum input voltage.

(2) Around GND terminal (GND terminal - C2(- side) - T1(D winding wire) - R2 – D2 - C2(+ side) - V_{IN} terminal)
This circuit also needs to be as wide and short as possible. In case the distance between C2 and the device is not short, placing a 0.1 – 1.0μF / 50V film capacitor between V_{IN} and GND terminals is recommended.

(3) Current Detection Resistance around R_{OCP}
Place R_{OCP} close to source (S) terminal.
In order to avoid the influence of common impedance or switching current on the control circuit, the main circuitry and control system ground should be connected near R_{OCP} and from R_{OCP} to the GND terminal by using the dedicated pattern (Position A in Fig. 8-7).

The typical connection of secondary side rectification is shown in Fig. 8-7.
(1) Secondary side rectifier smoothing circuit (T1 (S winding) – D3 – C7):
This pattern trace should be as thick and short as possible. If the rectification pattern is thin and long, the element of the parasitic leakage inductance is increased and the surge voltage at turn-off of MOSFET is increased.
The pattern design that the secondary side rectification pattern is taken into consideration achieves the wider withstand margin of power MOSFET and the reduction of stress and dissipation of the clamp snubber circuit.

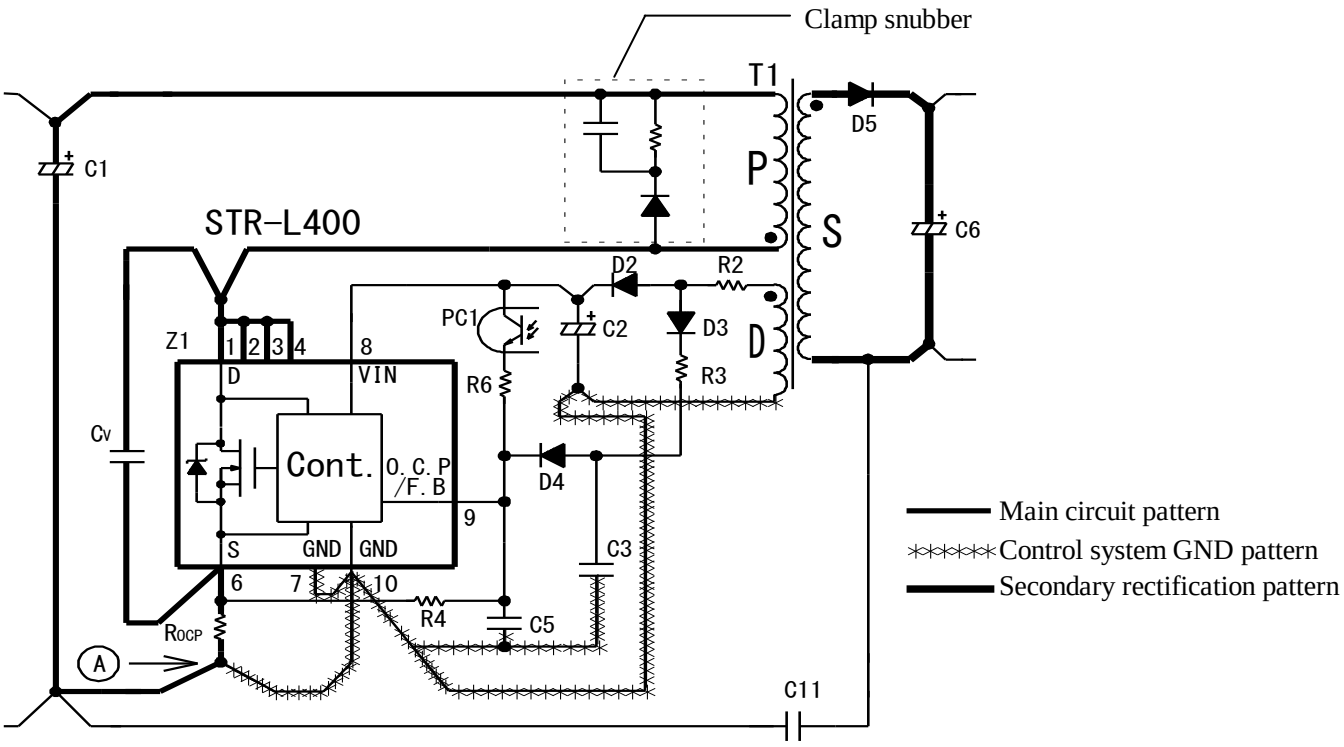


Fig. 8-7 Example of IC peripheral circuit connection