Sine-wave Driving, High Voltage 3-phase Motor Driver with Built-in Hall Amplifiers

SX68128MB

Data Sheet

Description

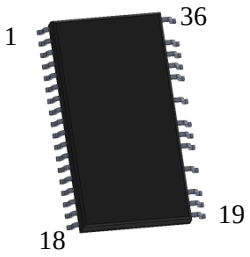
The SX68128MB is a high voltage 3-phase motor driver driven by a sinusoidal control, which can support Hall element and Hall IC inputs, thus offering high-efficient yet low-noise motor control. Supplied in a thin SOP36 package, where a controller, a gate driver, the output transistors of three phases, and bootstrap diodes are highly integrated, the SX68128MB requires only a few external components for building a motor driver. This also allows a motor driver to be highly reliable in performance and design-friendly with its compactness. The product can optimally control the inverter systems of low- to medium-capacity motors that require universal input standards.

Features

- Low Noise, High Efficiency (Sinusoidal Current Waveform)
- Reduced Number of Parts Achieved by Built-in Bootstrap Diodes with Current-limiting Resistors
- Pb-free (RoHS Compliant)
- Hall Element and Hall IC Inputs
- Rotation Pulse Signal FG Output (2.4 ppr)
- Application-specific Optimal Settings with External Signals:
  - Motor Speed
  - Phase Adavance Angle
  - Motor Direction
  - User-settable Motor Lock Detection (Enabled or Disabled)
- 5 V Reference Voltage Output (Used for Driving Hall Elements etc.)
- Fault Signal Output at Protection Activation (FO Pin)
- Protections Include:
  - VREG Pin Undervoltage Lockout (UVLO_VREG)
  - Undervoltage Lockout for Power Supplies
    VBx Pin (UVLO_VB)
    VCC1 Pin (UVLO_VCC)
  - Overcurrent Limit (OCL)
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - Motor Lock Protection (MLP)
  - Reverse Rotation Detection
  - Hall Signal Abnormality Detection

Package

SOP36



Not to scale

Specifications

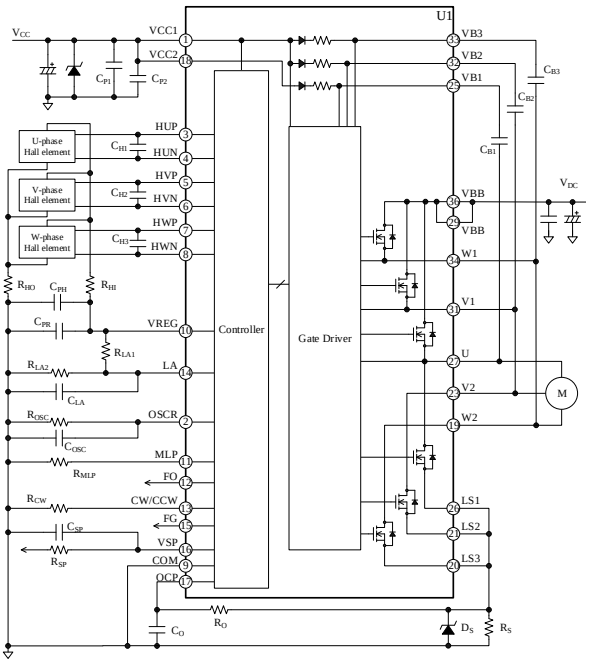
- V_{DSS} : 600 V
- I_O: 1.5 A
- $R_{DS(ON)}$ (max.): 3.6 Ω

Applications

For motor drives such as:

- Fan Motor for Air Conditioner
- Fan Motor for Air Purifier and Electric Fan

Typical Application



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1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C.

Parameter	Symbol	Conditions	Rating	Unit
Power MOSFET Breakdown Voltage	V_{DSS}	I_D = 100 µA	600	V
Logic Supply Voltage	V_{CC}	VCCx–COM	20	V
	V_{BS}	VB1–U, VB2–V1, VB3–W1	20	
Output Current (DC)(1)	I_O	T_C = 25 °C, T_J < 150 °C	1.5	A
Output Current (Pulse)	I_{OP}	T_C = 25 °C, pulse width ≤ 100 µs	2.25	A
VREG Pin Voltage	V_{REG}		5.5	V
VREG Pin Current	I_{REG}		30	mA
Input Voltage 1 (HUP, HUN, HVP, HVN, HWP, HWN)	$V_{IN(1)}$		−0.5 to V_{REG}	V
Input Voltage 2 (OSCR, MLP, CW/CCW, LA, OCP)	$V_{IN(2)}$		−0.5 to V_{REG}	V
Input Voltage 3 (VSP)	$V_{IN(3)}$		−0.5 to 10	V
Output Voltage (FG, FO)	V_O		−0.5 to V_{REG}	V
LSx Pin Voltage (DC)	$V_{LS(DC)}$	LSx–COM	−0.7 to 7	V
LSx Pin Voltage (Surge)	$V_{LS(SURGE)}$	LSx–COM	−4 to 7	V
Allowable Power Dissipation	P_D	T_C = 25 °C	3.5	W
Operating Case Temperature(2)	$T_{C(OP)}$		−30 to 100	°C
Junction Temperature(3)	T_J		150	°C
Storage Temperature	T_{STG}		−40 to 150	°C

(1) Should be derated depending on an actual case temperature. See Section 13.4.
(2) Refers to a case temperature measured during IC operation.
(3) Refers to the junction temperature of each chip built in the IC, including the control stage, gate drive stage, power MOSFETs, and bootstrap diodes.

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2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Main Supply Voltage	V_{DC}	VBB–LSx	—	300	400	V
Logic Supply Voltage	V_{CC}	VCCx–COM	13.5	—	16.5	V
	V_{BS}	VB1–U, VB2–V1, VB3–W1	13.5	—	16.5	V
Input Voltage 1 (HUP, HUN, HVP, HVN, HWP, HWN)	$V_{IN(1)}$		0	—	5.0	V
Input Voltage 2 (MLP, CW/CCW)	$V_{IN(2)}$		0	—	5.0	
Input Voltage 3 (VSP)	$V_{IN(3)}$		0	—	5.4	V
FO Pin Noise Filter Capacitor	C_{FO}		0.001	—	0.01	μF
Bootstrap Capacitor	C_B		1	—	—	μF
Shunt Resistor*	R_S	$I_{OP} \leq 2.25$ A	0.4	—	—	Ω
RC Filter Resistor	R_O		—	—	100	Ω
RC Filter Capacitor	C_O		100	—	2200	pF
Operating Case Temperature	$T_{C(OP)}$		—	—	100	°C

* Should be a resistor with low inductance.

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3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−). Unless specifically noted, T_A = 25 °C, V_{CC} = 15 V.

3.1 Characteristics of Control Parts

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Operation						
Low-side Logic Operation Start Voltage	$V_{CC(ON)}$	VCCx–COM	10.5	11.5	12.5	V
Low-side Logic Operation Stop Voltage	$V_{CC(OFF)}$		10.0	11.0	12.0	V
High-side Logic Operation Start Voltage	$V_{BS(ON)}$	VB1–U, VB2–V1, VB3–W1	9.5	10.5	11.5	V
High-side Logic Operation Stop Voltage	$V_{BS(OFF)}$		9.0	10.0	11.0	V
Logic Supply Current	I_{CC}	V_{SP} = 5.4 V, I_{REG} = 0 A	—	6	10	mA
	I_{BS}	V_{Bx} = 15 V, V_{SP} = 5.4 V; VBx pin current in 1-phase operation	—	90	250	µA
Input Signal						
High Level Input Voltage[1] (MLP, CW/CCW)	V_{IH}		3.4	—	—	V
Low Level Input Voltage (MLP, CW/CCW)	V_{IL}		—	—	1.6	V
High Level Input Current 1 (MLP, CW/CCW, LA, VSP)	I_{IH1}	V_{IN} = V_{REG}	—	30	100	µA
Low Level Input Current 1 (MLP, CW/CCW, LA, VSP)	I_{IL1}	V_{INL} = 0 V	—	—	2	µA
High Level Input Current 2 (OCP)	I_{IH2}	V_{IN} = V_{REG}	−5	—	5	µA
Low Level Input Current 2 (OCP)	I_{IL2}	V_{INL} = 0 V	—	23	90	µA
FG Pin High Level Output Voltage	V_{OH}		4.5	—	5.5	V
FG Pin Low Level Output Voltage	V_{OL}		—	—	0.5	V
FO Pin High Level Output Voltage	$V_{FO(H)}$		4.5	—	5.5	V
PWM Control						
PWM Carrier Frequency[2]	f_C	OSCR = Open	16	17	18	kHz
Internal Oscillator Frequency[2]	f_{OSC}		4.10	4.32	4.54	MHz
Dead Time[2]	t_D		—	1.2	—	µs
Control IC Output Pulse Duty Cycle[2]	D	V_{SP} = 2.0 V	—	0	3	%
		V_{SP} = 3.75 V	47	50	53	%
		V_{SP} = 5.4 V (driven by sinusoidal control)	93.7	—	100	%
Protection						
OCL Threshold Voltage	V_{LIM}		0.46	0.50	0.54	V
OCL Blanking Time	$t_{BK(OCL)}$	OSCR = Open	—	1.9	—	µs
OCP Threshold Voltage	V_{TRIP}		0.7	0.8	0.9	V
OCP Blanking Time	$t_{BK(OCP)}$	OSCR = Open	—	1.3	—	µs

[1] Guaranteed by design.
[2] Refers to an internal signal; guaranteed by design.

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Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
OCP Hold Time	t_P	OSCR = Open	—	15	—	ms
MLP Detection Time	t_{LD}	OSCR = Open	—	6	—	s
MLP Hold Time	t_{LH}	OSCR = Open	—	35	—	s
TSD Operating Temperature(3)	T_{DH}	I_{REG} = 0 mA; without heatsink	—	130	—	°C
TSD Releasing Temperature(3)	T_{DL}		—	90	—	°C
TSD Hysteresis Temperature(3)	$T_{D(HYS)}$		—	40	—	°C
VREG Pin Output Voltage	V_{REG}	I_{REG} = 0 mA to 30 mA	4.5	5.0	5.5	V
VREG Pin Undervoltage Lockout Operating Voltage(2)	V_{UVRL}		—	3.6	—	V
VREG Pin Undervoltage Lockout Releasing Voltage(2)	V_{UVRH}		—	4.0	—	V

(3) Refers to the junction temperature of the gate drive stage.

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3.2 Transistor Characteristics

Figure 3-1 provides the definitions of switching characteristics described in this and the following sections. V_{GS} represents the voltage between the gate and source of an internal power MOSFET.

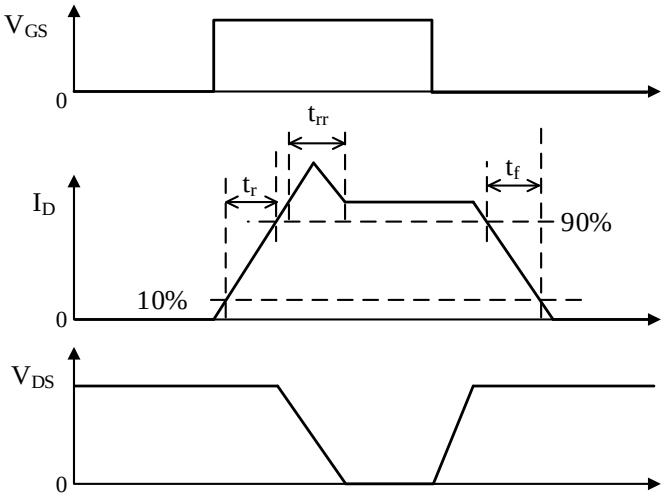

Figure 3-1. Switching Characteristics Definitions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V	—	—	100	μA
Drain-to-Source On-resistance	$R_{DS(ON)}$	I_D = 0.75 A	—	2.9	3.6	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} = 0.75 A	—	0.95	1.5	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time*	t_{rr}	V_{DC} = 300 V, V_{CC} = 15 V, I_D = 0.75 A, V_{GS} = 0→15 V or 15→0 V, T_J = 25 °C, inductive load	—	125	—	ns
Rise Time*	t_r		—	60	—	ns
Fall Time*	t_f		—	25	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time*	t_{rr}	V_{DC} = 300 V, V_{CC} = 15 V, I_D = 0.75 A, V_{GS} = 0→15 V or 15→0 V, T_J = 25 °C, inductive load	—	130	—	ns
Rise Time*	t_r		—	65	—	ns
Fall Time*	t_f		—	30	—	ns

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3.3 Bootstrap Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Bootstrap Diode Leakage Current	I_{LBD}	V_R = 600 V	—	—	10	μA
Bootstrap Diode Forward Voltage	V_{FB}	I_{FB} = 0.15 A; R_{BOOT} excluded	—	1.0	1.3	V
Bootstrap Diode Series Resistor	R_{BOOT}		45	60	75	Ω

3.4 Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Junction-to-Case Thermal Resistance(1)	R_{J-C}	All power MOSFETs operating(2)	—	—	10	°C/W
Junction-to-Ambient Thermal Resistance	R_{J-A}	All power MOSFETs operating(2)	—	—	35	°C/W

(1) Refers to a case temperature at the measurement point described in Figure 3-2.
(2) Mounted on a CEM-3 glass (1.6 mm in thickness, 35 μm in copper foil thickness), and measured under natural air cooling without silicone potting.

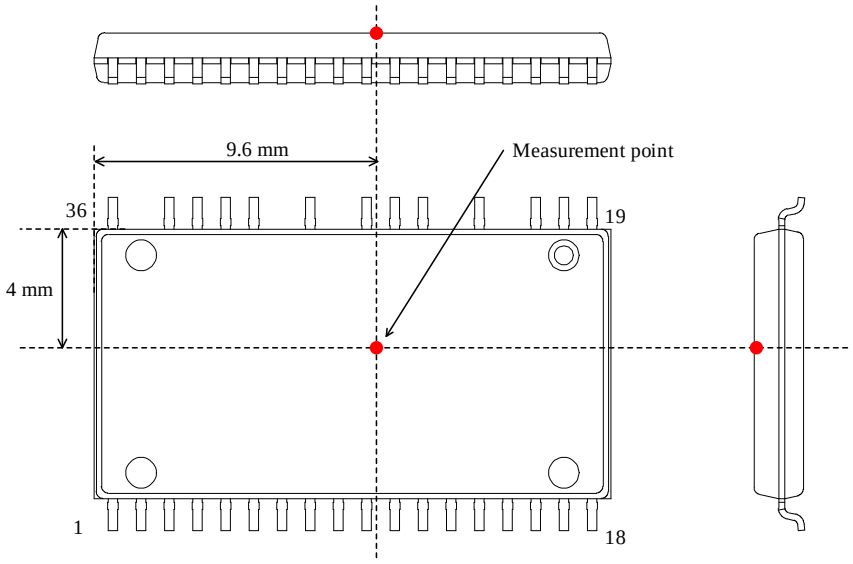

Figure 3-2. Case Temperature Measurement Point

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4. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Package Weight		—	1.4	—	g

5. Block Diagram

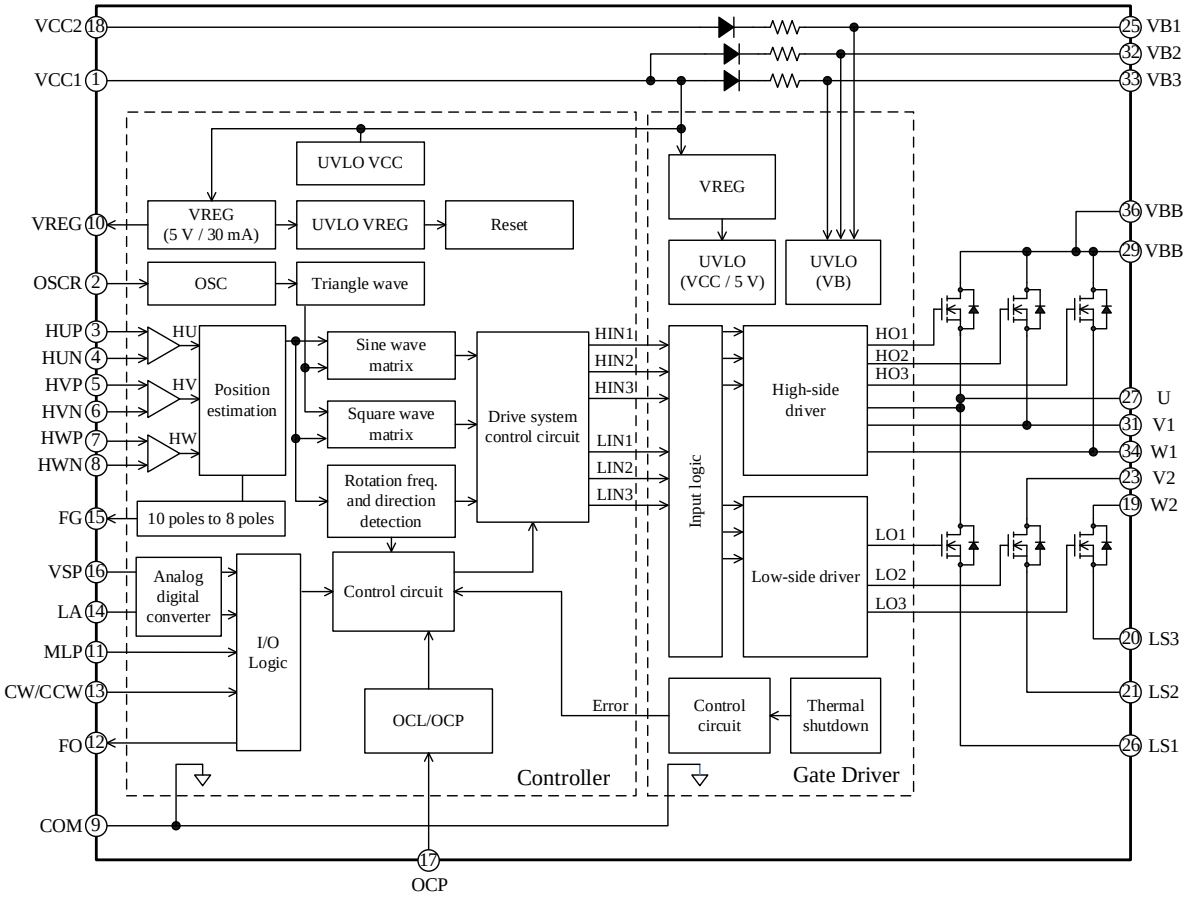

Figure 5-1. Block Diagram

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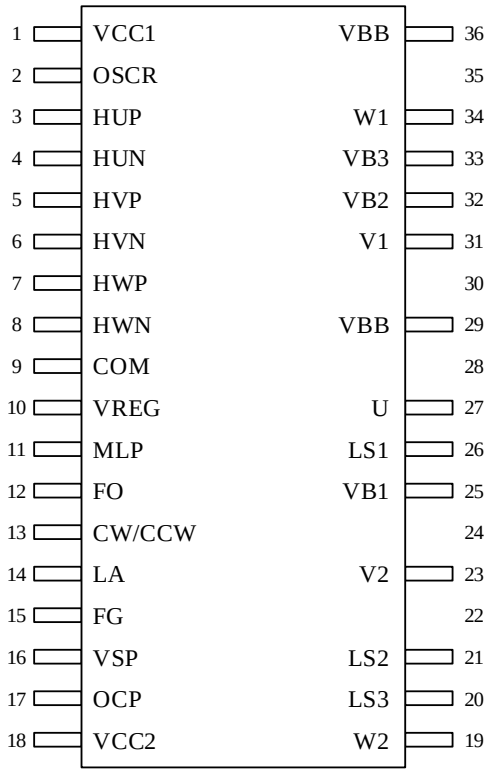
6. Pin Configuration Definitions

Top View



Pin Number	Pin Name	Description
1	VCC1	Logic supply voltage input 1
2	OSCR	Input for oscillator frequency setting signal
3	HUP	U-phase Hall element positive signal input (+)
4	HUN	U-phase Hall element negative signal input (−)
5	HVP	V-phase Hall element positive signal input (+)
6	HVN	V-phase Hall element negative signal input (−)
7	HWP	W-phase Hall element positive signal input (+)
8	HWN	W-phase Hall element negative signal input (−)
9	COM	Logic ground
10	VREG	Internal regulator output
11	MLP	Setting pin to enable or disable the motor lock protection
12	FO	Fault signal output
13	CW/CCW	Input for motor direction setting signal
14	LA	Input for phase advance angle setting signal
15	FG	Rotation pulse signal output (2.4 ppr)
16	VSP	Input for motor speed control signal
17	OCP	Input for overcurrent detection signal
18	VCC2	Logic supply voltage input 2
19	W2	W-phase output (connected to W1 externally)
20	LS3	W-phase low-side power MOSFET source
21	LS2	V-phase low-side power MOSFET source
22	—	Pin removed
23	V2	V-phase output (connected to V1 externally)
24	—	Pin removed
25	VB1	U-phase high-side floating supply voltage input
26	LS1	U-phase low-side power MOSFET source
27	U	U-phase output
28	—	Pin removed
29	VBB	Positive DC bus supply voltage (+)
30	—	Pin removed
31	V1	V-phase output (connected to V2 externally)
32	VB2	V-phase high-side floating supply voltage input
33	VB3	W-phase high-side floating supply voltage input
34	W1	W-phase output (connected to W2 externally)
35	—	Pin removed
36	VBB	Positive DC bus supply voltage (+)

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7. Typical Applications

Figure 7-1 is a typical application which uses signals input from the Hall elements; Figure 7-2 is a typical application which uses signals input from Hall ICs.

CR filters and Zener diodes should be added to your application as needed. This is to protect each pin against surge voltages causing malfunctions, and to avoid the IC being used under the conditions exceeding the absolute maximum ratings where critical damage is inevitable. Then, check all the pins thoroughly under actual operating conditions to ensure that your application works flawlessly.

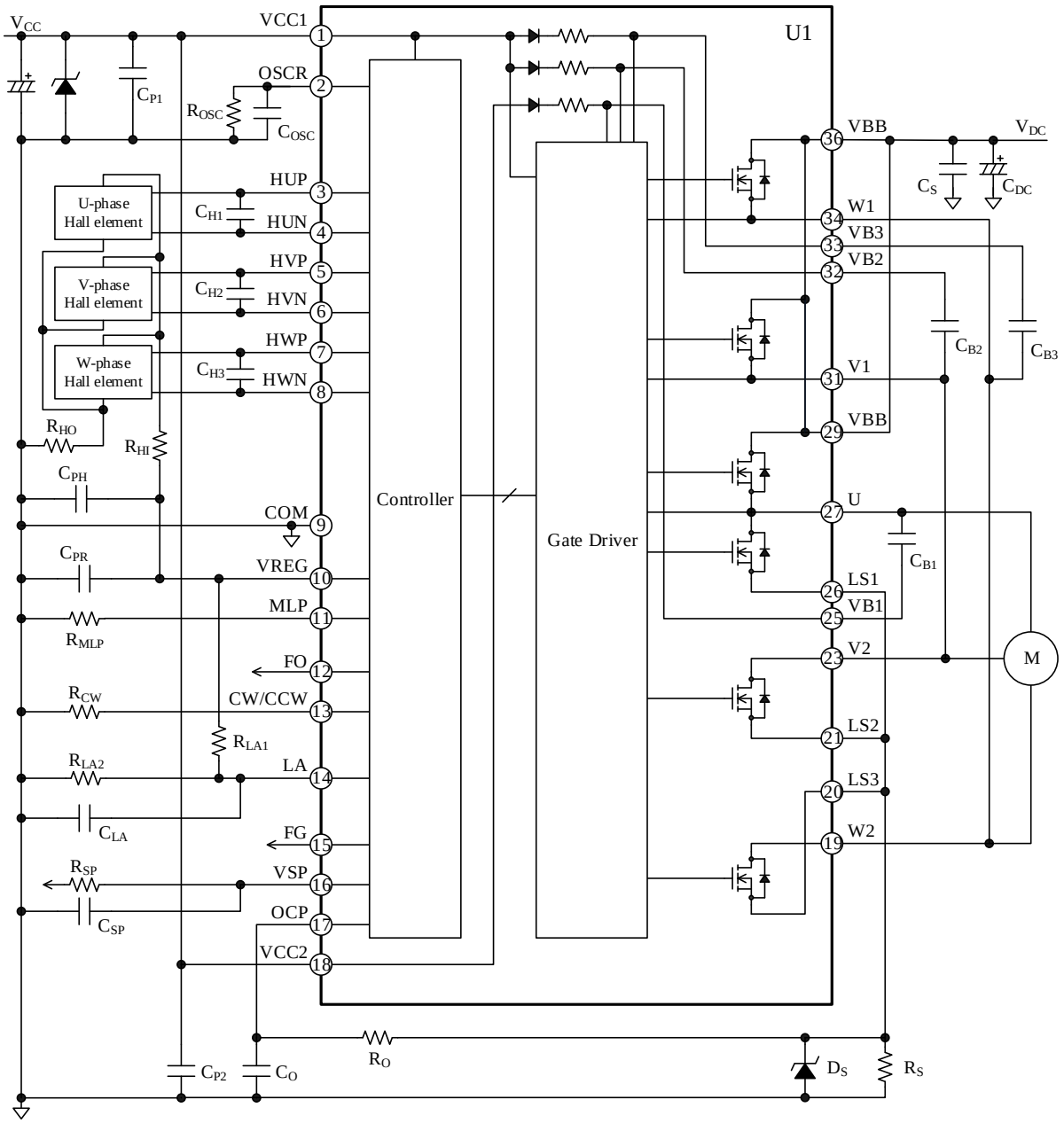

Figure 7-1. Application Using Signals Input from Hall Elements

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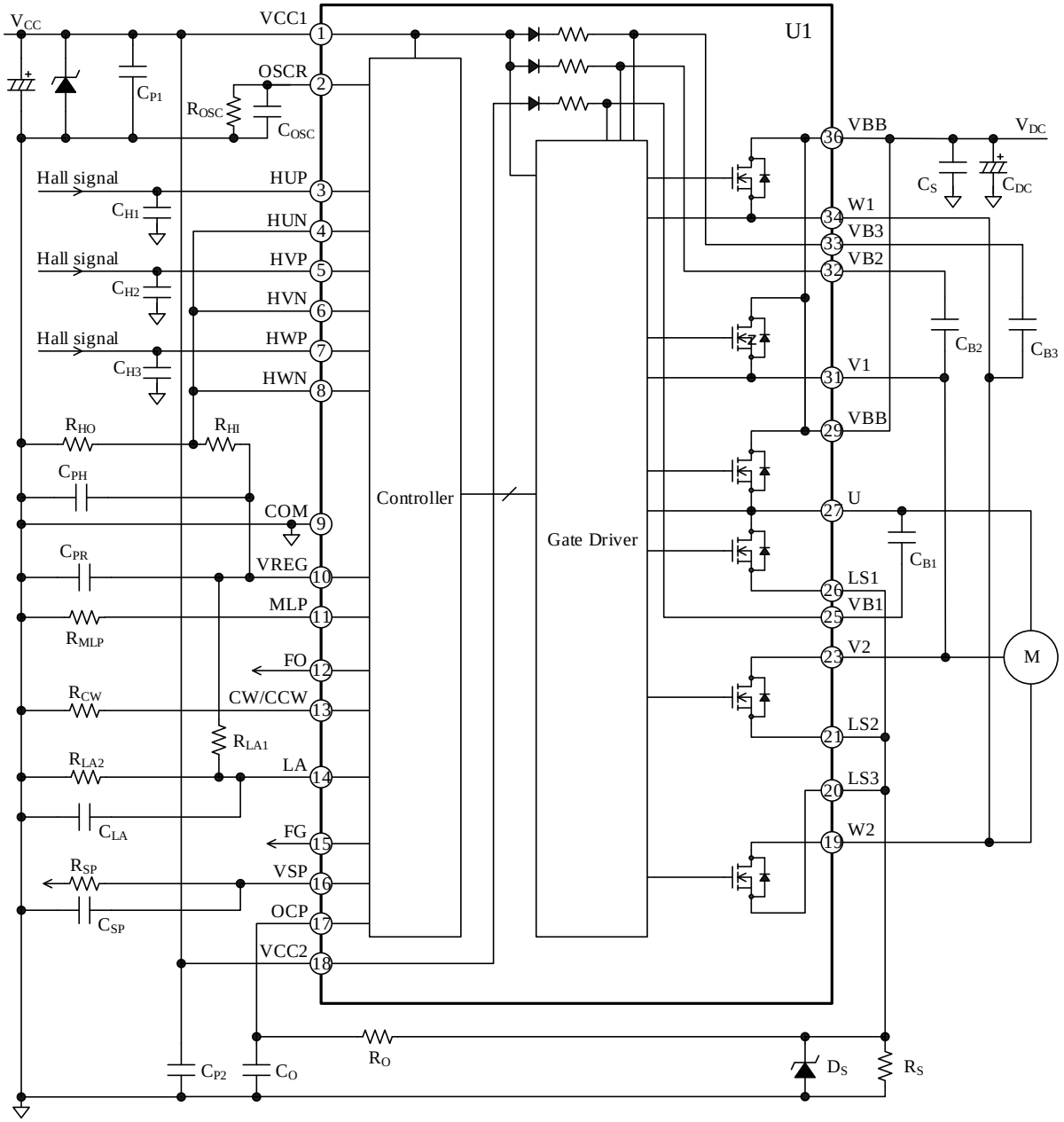

Figure 7-2. Application Using Signals Input from Hall ICs

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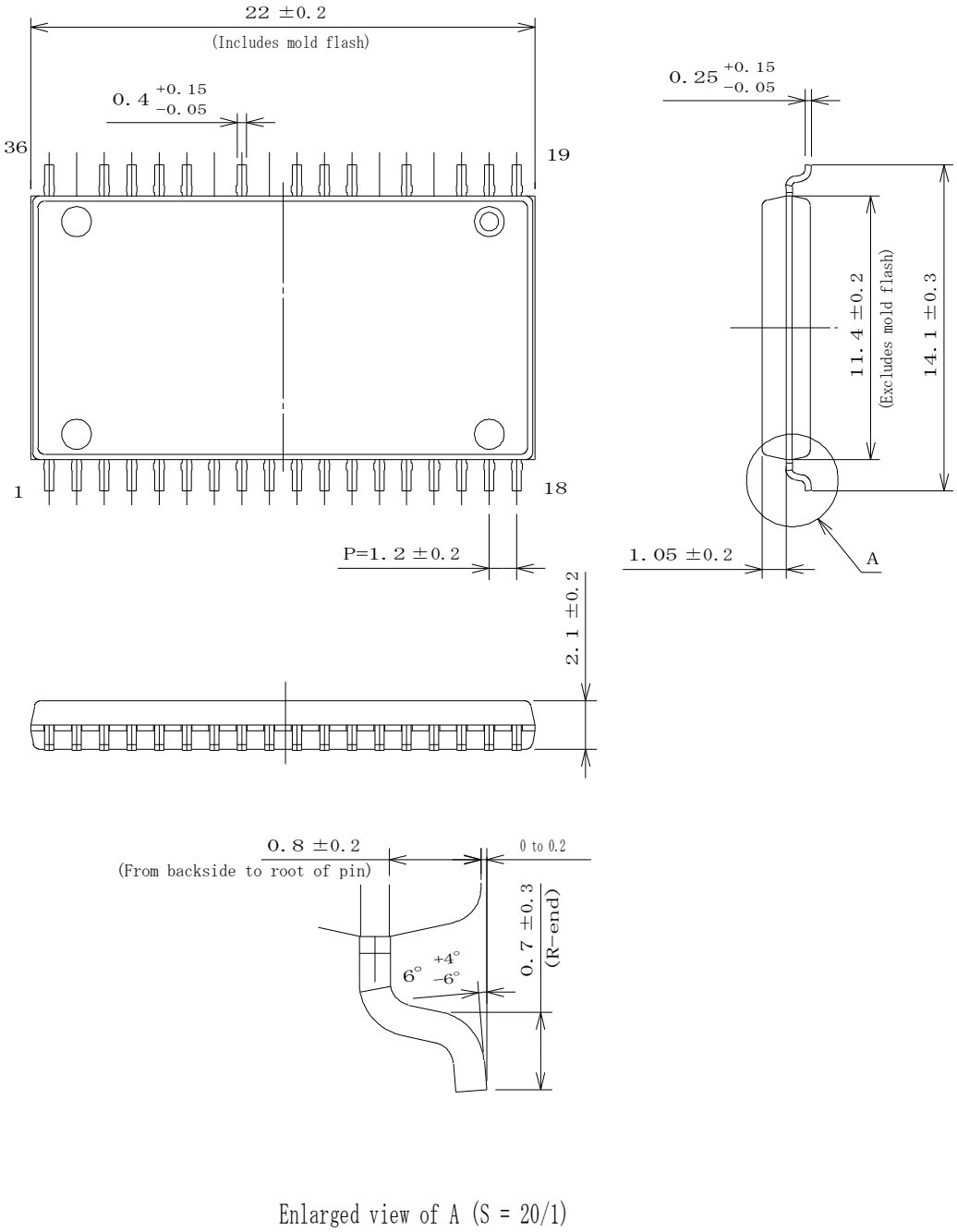
8. Physical Dimensions

● **SOP36 Package**



Enlarged view of A (S = 20/1)

NOTES:

- Dimensions in millimeters
- Pb-free (RoHS compliant)
- When soldering the products, it is required to minimize the working time, within the following limits:
  Reflow (MSL3):
  Preheating: 180 °C / 90 ± 30 s
  Solder heating: 250 °C / 10 ± 1 s (260 °C peak, 2 times)
  Soldering iron: 380 ± 10 °C / 3.5 ± 0.5 s, 1 time

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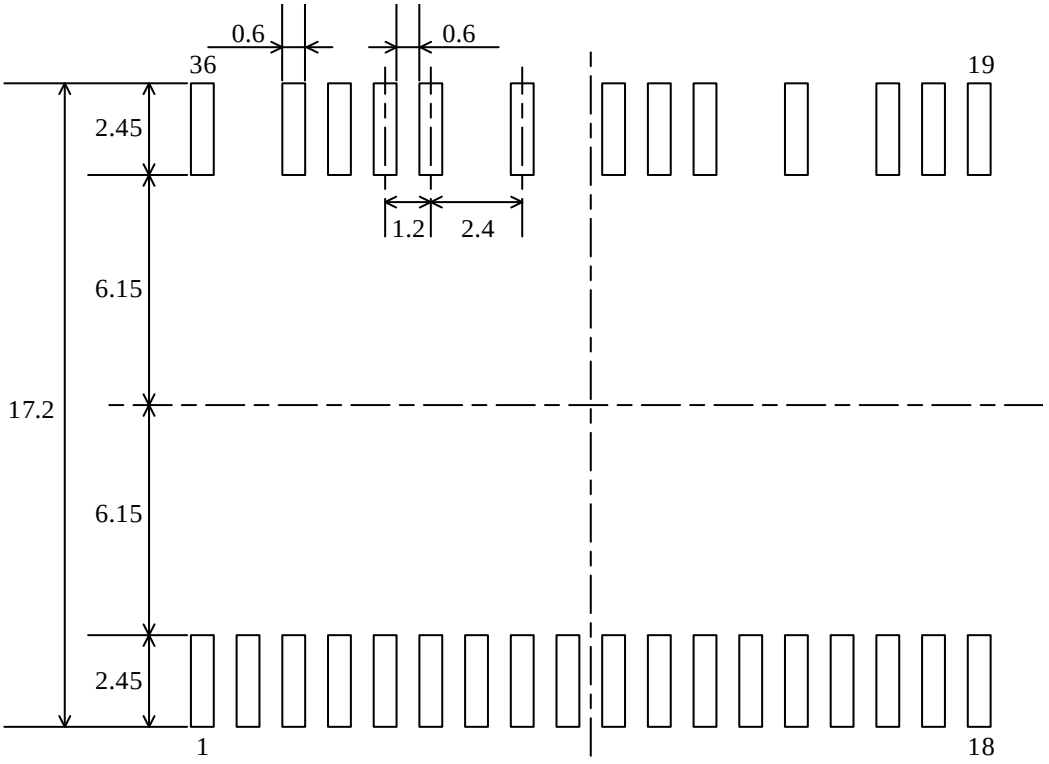
● **Land Pattern Example**



Unit: mm

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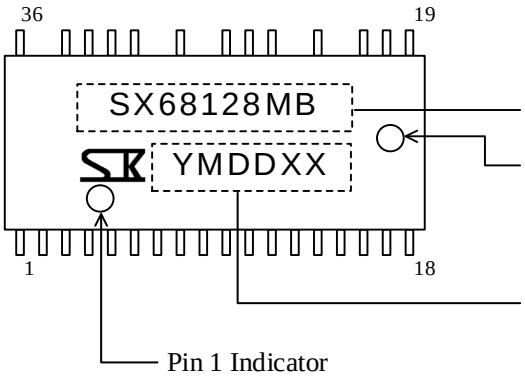
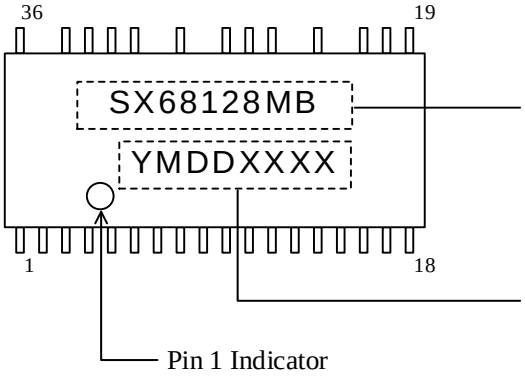
9. Marking Diagram

● **Type A**



● **Type B**



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10. Functional Descriptions

For concise descriptions, this section employs notation systems that denote the electrical characteristics symbols listed in Section 3 and the electronic symbol names of the typical applications in Section 7. All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum. For pin and peripheral component descriptions, this section employs a notation system that denotes a pin name or an electronic symbol name with the arbitrary letter "x", representing the certain numbers and letters (1 to 3 and U to W). Thus, "the VCCx pin" is used when referring to either or both of the VCC1 and VCC2 pins.

10.1 Pin Descriptions

10.1.1 VCC1 and VCC2

These are the logic supply pins for the built-in control IC. The VCC1 pin has the undervoltage lockout for power supply (see Section 10.7.2.2). The VCC1 and VCC2 pins must be externally connected on a PCB because they are not internally connected. To prevent malfunction induced by supply ripples or other factors, put a 0.01 µF to 0.1 µF ceramic capacitor, C_{Px}, near these pins. To prevent damage caused by surge voltages, put an 18 V to 20 V Zener diode, DZ, between the VCCx and COM pins. Voltages to be applied between the VCCx and COM pins should be regulated within the recommended operational range of V_{CC}, given in Section 2.

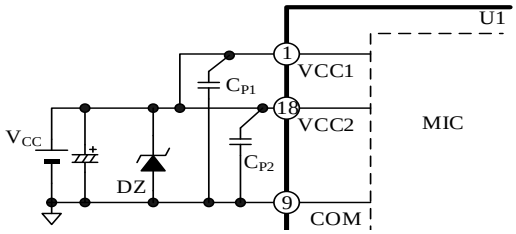

Figure 10-1. VCCx Pin Peripheral Circuit

10.1.2 OSCR

Figure 10-2 shows the OSCR pin and its peripheral circuit. To adjust a frequency of the internal oscillator, connect a resistor, R_{OSC}, to the OSCR pin. To reduce noises on the pin, connect a noise filter capacitor, C_{OSC}, with a capacitance of about 0.1 µF. Figure 10-3 shows how the carrier frequency, f_{PWM}, and the resistance, R_{OSC}, are related. When the OSCR pin is open, the carrier frequency is set to f_C = 17 kHz. The following characteristics depend on a frequency of the internal oscillator:

- OCP Hold Time, t_P
- OCL Blanking Time, $t_{BK(OCL)}$
- OCP Blanking Time, $t_{BK(OCP)}$
- MLP Detection Time, t_{LD}
- MLP Hold Time, t_{LH}

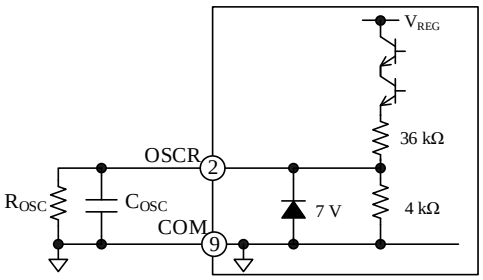

Figure 10-2. Internal Circuit Diagram of OSCR Pin and Its Peripheral Circuit

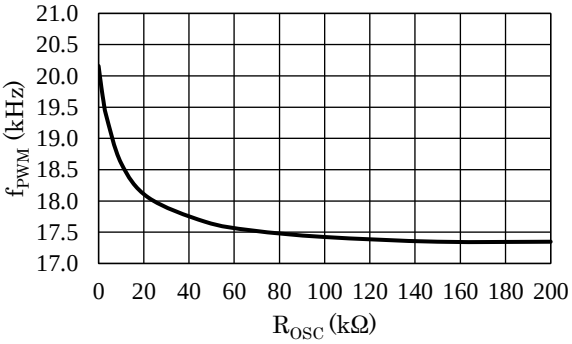

Figure 10-3. Typical Performance Curve of OSCR Pin

10.1.3 HUP, HVP, and HWP; HUN, HVN, and HWN

These are the input pins for Hall element signals. The HxP pin is connected to the positive node of a Hall element, whereas the HxN pin is connected to the negative node of a Hall element. As Figure 10-4 illustrates, connect a noise filter capacitor, C_{Hx}, with a capacitance of about 0.1 µF, between the HxP and HxN pins. C_{Hx} must be placed near the IC with a minimal length of traces. The IC incorporates the protection circuit that detects abnormal signals from the external Hall elements (see Section 10.7.7).

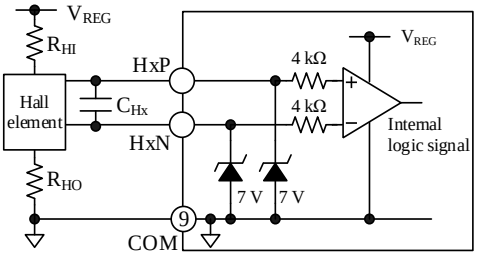

Figure 10-4. Internal Circuit Diagram of HxP and HxN Pins and Their Peripheral Circuit

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10.1.4 COM

This is the logic ground pin for the built-in control ICs. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect the logic ground as close and short as possible to a shunt resistor, R_S, at a single-point ground (or star ground) which is separated from the power ground (see Figure 10-5).

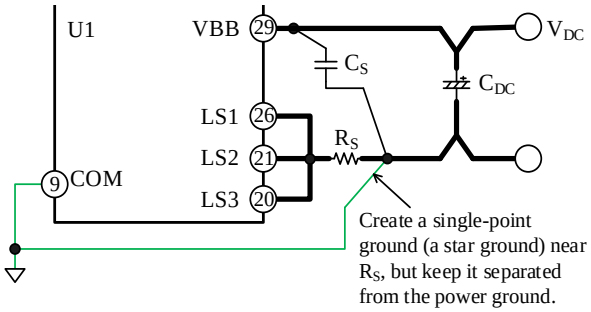

Figure 10-5. Connections to Logic Ground

10.1.5 VREG

This is the 5.0 V regulator output pin, which can be used for the power supply of the external Hall elements. A maximum output current of the VREG pin is 30 mA. To stabilize the VREG pin output, connect a capacitor, C_{PR}, of about 0.1 µF to the pin. The VREG pin also has the undervoltage lockout. For more details on this function, see Section 10.7.1.

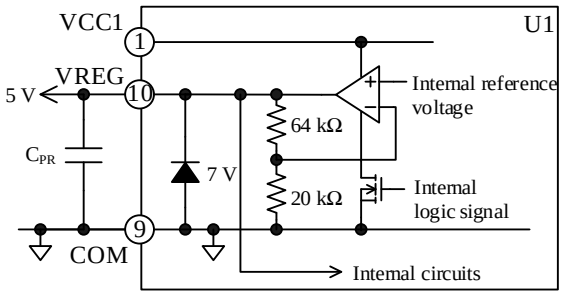

Figure 10-6. Internal Circuit Diagram of VREG Pin

10.1.6 MLP

The IC determines to enable or disable the motor lock protection based on the setting of this pin. Table 10-1 provides the logic level definitions for the MLP pin. The IC detects which logic level the MLP pin has been set during a startup period (i.e., when the VCCx pin voltage is rising).

Figure 10-7 shows an internal circuit diagram of the MLP pin. To set the MLP pin to logic low, leave the pin open. To set the MLP pin to logic high, connect the pin to the VREG pin. Section 10.7.5 explains more details on the motor lock protection.

Table 10-1. Logic Levels Defined for MLP Pin

MLP Pin	MLP Setting Status
L	Enabled
H	Disabled

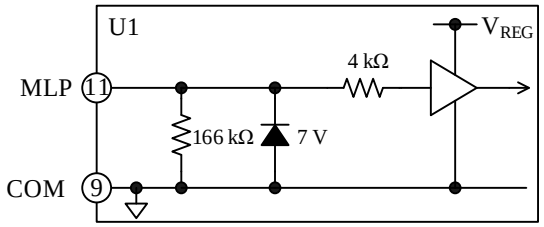

Figure 10-7. Internal Circuit Diagram of MLP Pin

10.1.7 FO

This pin operates as the fault signal output. For more details on the fault signal output, see Section 10.6. Figure 10-8 shows an internal circuit diagram of the FO pin. The FO pin is internally connected to the drains of the P-channel power MOSFET. The FO pin can also be directly connected to the input pin of the external microcontroller. For avoiding repeated OCP activations, the external microcontroller must shut off any input signals to the IC within an OCP hold time, t_P = 15 ms, after a fault signal output. (For more details, see Section 10.7.3.)

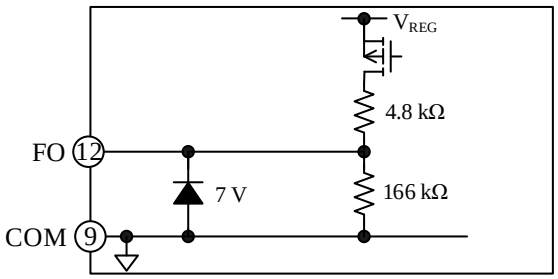

Figure 10-8. Internal Circuit Diagram of FO Pin

10.1.8 CW/CCW

This is the setting pin which determines the direction of motor rotation. Table 10-2 lists the logic level definitions for the CW/CCW pin and the corresponding motor directions. And Figure 10-9 shows an internal circuit diagram of the CW/CCW pin. To set the CW/CCW pin to logic low, connect the pin to the GND pin. To set the CW/CCW pin to logic high, connect the pin to the VREG pin. The IC detects which logic level the CW/CCW pin has been set during a startup period

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(i.e., a period during which the VCCx pin voltage is rising). After the startup period ends, the IC constantly monitors the logic state of the CW/CCW pin.

Table 10-2. Logic Levels Defined for CW/CCW Pin

CW/CCW Pin	Motor Direction
L	Reverse (CCW)
H	Forward (CW)

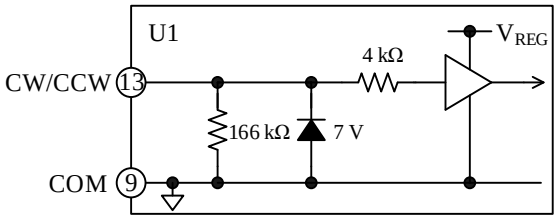

Figure 10-9. Internal Circuit Diagram of CW/CCW Pin

10.1.9 LA

The IC features the phase advance function. The angle of phase advance is determined by an analog voltage applied to the LA pin. Section 10.5 gives detailed explanations on the LA pin settings and the phase advance function.

10.1.10 FG

The FG pin outputs a rotation pulse signal that is generated based on a position sensing signal (2.4 ppr). A rotation pulse signal is inverted at each edge of the Hall element signal assigned to the U-, V-, and W-phases. As shown in Figure 10-10, the FG pin is internally pulled down to the COM pin.

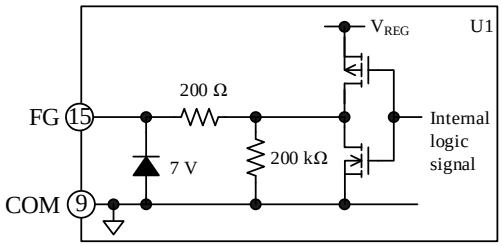

Figure 10-10. Internal Circuit Diagram of FG Pin

10.1.11 VSP

The IC controls the speed of motor rotation with an analog voltage applied to the VSP pin. For more details on the motor speed control, see Section 10.4.

10.1.12 OCP

This pin serves as the input of the overcurrent protection (OCP) which monitors the currents flowing through the output transistors. The IC determines which of the overcurrent limit (OCL) and overcurrent protection (OCP) functions to activate according to the level of a voltage applied to the OCP pin. Section 10.7.3 provides further information about the OCP circuit configuration and its mechanism.

10.1.13 VBB

This is the input pin for the main supply voltage, i.e., the positive DC bus. All of the power MOSFET drains of the high-side are connected to this pin. Voltages between the VBB and COM pins should be set within the recommended range of the main supply voltage, V_{DC}, given in Section 2.

To suppress surge voltages, put a 0.01 µF to 0.1 µF bypass capacitor, C_S, near the VBB pin and an electrolytic capacitor, C_{DC}, with a minimal length of PCB traces to the VBB pin.

10.1.14 VB1, VB2, and VB3

The VB1, VB2, and VB3 pins are connected to bootstrap capacitors, C_{Bx}, for the high-side floating supply. For proper startup, turn on the low-side transistors first, then fully charge the bootstrap capacitors, C_{Bx}.

For the capacitance of the bootstrap capacitors, C_{Bx}, choose the values that satisfy Equations (1) and (2). Note that capacitance tolerance and DC bias characteristics must be taken into account when you choose appropriate values for C_{Bx}.

$$C_{Bx}(\mu F) > 800 \times t_{L(OFF)} \quad (1)$$

$$1\ \mu F \leq C_{Bx} \leq 220\ \mu F \quad (2)$$

In Equation (1), let $t_{L(OFF)}$ be the maximum off-time of the low-side transistor (i.e., the non-charging time of C_{Bx}), measured in seconds.

Even while the high-side transistor is off, voltage across the bootstrap capacitor keeps decreasing due to power dissipation in the IC. When the VBx pin voltage decreases to $V_{BS(OFF)}$ or less, the high-side undervoltage lockout (UVLO_VB) starts operating (see Section 10.7.2.1). Therefore, actual board checking should be done thoroughly to validate that voltage across the VBx pin maintains over 11.0 V ($V_{BS} > V_{BS(OFF)}$) during a low-frequency operation such as a startup period.

As Figure 10-11 shows, a bootstrap diode, D_{BOOTx}, and a current-limiting resistor, R_{BOOTx}, are internally

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placed in series between the VCCx and VBx pins. Time constant for the charging time of C_{Bx}, τ, can be computed by Equation (3):

$$\tau = C_{Bx} \times R_{BOOTx}\ , \qquad (3)$$

where C_{Bx} is the optimized capacitance of the bootstrap capacitor, and R_{BOOTx} is the resistance of the current-limiting resistor (60 Ω ± 20%).

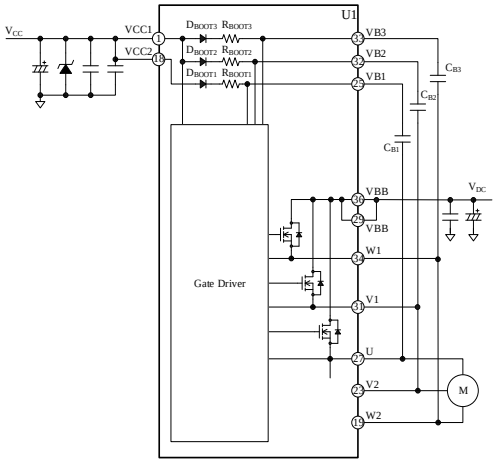

Figure 10-11. Bootstrap Circuit

Section 10.2 describes the startup sequences of the IC in detail; Section 10.3 explains the procedures to charge the bootstrap capacitors.

C_{Bx} ,with a capacitance of about 1 μF, must be placed near the IC, and connected between VBx and output (U, V1, W1) pins with a minimal length of trances.

10.1.15 U, V1, V2, W1, and W2

These pins are the outputs of the three phases, and serve as the connection terminals to the 3-phase motor. The V1 and W1 pins must be connected to the V2 and W2 pins on a PCB, respectively. The U, V, and W1 pins are the grounds for the VB1, VB2, and VB3 pins. The U, V1, and W1 pins are connected to the negative nodes of bootstrap capacitors, C_{Bx}. Since high voltages are applied to these output pins (U, V1, V2, W1, W2), it is required to take measures for insulating as follows:

- Keep enough distance between the output pins and low-voltage traces.
- Coat the output pins with insulating resin.

10.1.16 LS1, LS2, and LS3

The LS1, LS2, and LS3 pins are internally connected to the low-side power MOSFET sources of the U-, V-, and W-phases, respectively. The LSx pin should be connected to an external shunt resistor, R_S, on a PCB. When connecting the shunt resistor, use the resistor with low inductance (required), and place it as near as possible to the IC with a minimum length of traces to the LSx and COM pins. Otherwise, malfunction may occur because a longer circuit trace increases its inductance and thus increases its susceptibility to improper operations. In applications where long PCB traces are required, add a fast recovery diode, D_{RS}, between the LSx and COMx pins in order to prevent the IC from malfunctioning.

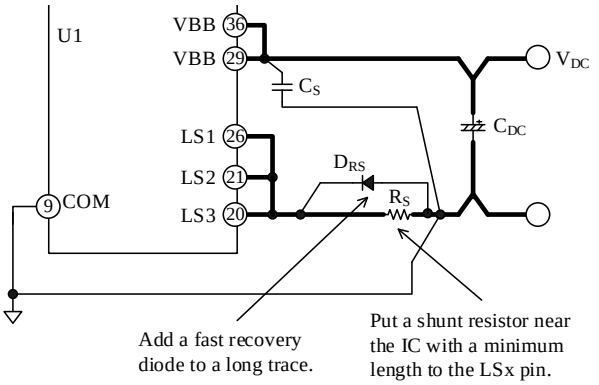

Figure 10-12. Connections to LSx Pin

10.2 Startup Operation

When the VCCx pin voltage reaches $V_{CC(ON)}$ = 11.5 V, the IC starts operating. As the startup sequence starts, the IC detects and reflects the logic states of the following pins to the motor control settings: the MLP pin for enabling or disabling the motor lock protection; the CW/CCW pin for setting the motor direction. The IC then waits for the VSP pin voltage to reach a certain level at which output duty cycles are controllable. At startup, the IC operates according to the VSP pin voltage levels as follows:

- **V_{SP} < 1.0 V:**
  All the output signals are off.

- **1.0 V ≤ V_{SP} < 2.1 V:**
  The IC starts charging bootstrap capacitors. For more details, see Section 10.3.

- **2.1 V ≤ V_{SP} ≤ 5.4 V:**
  The IC controls its output duty cycles according to the VSP pin voltage levels. While the frequency of a position sensing signal, Hx, is less than 1.0 Hz at startup, the motor is driven by a trapezoidal control. When Hx increases to 1.0 Hz or more (i.e., the condition in which a position sensing signal is detected at every rotation of 60° in electrical degrees), the IC generates a sine-wave signal and drives the motor by a sinusoidal control.

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Table 10-3 and Table 10-4 are truth tables for the motor driven by the trapezoidal control in a forward or reverse rotation. Moreover, the timing charts shown later represent the operational waveforms in the following motor operations: the motor in a forward rotation (no phase advance; Figure 10-17), the motor in a forward rotation (phase advance by 15°; Figure 10-18), and the motor in a reverse rotation (Figure 10-19). The following symbols used in Figure 10-17 to Figure 10-19 represent the signals generated inside the IC: S_U, S_V, S_W, S_X, S_Y, S_Z.

When the IC detects a state in which the motor rotates inversely to the preset direction, the motor driving system is immediately switched to the trapezoidal control before a rotation of 60° electrical angle completes. For detailed descriptions on the reverse rotation detection, see Section 10.7.6.

The following are the important considerations for appropriate power startup and shutdown sequences.

- To turn on the IC, be sure to increase the VSP pin voltage last. To turn off the IC, be sure to decrease the VSP pin voltage first.
- When you have enabled the motor lock protection (MLP = L), be sure to apply a voltage to the VBB pin at the timing described below. At startup, apply a voltage to the VCCx pin and the VREG pin voltage, V_{REG}, increases. Then, apply a main supply voltage to the VBB pin within the period from V_{REG} increase to an MLP detection time, t_{LD}. When a position sensing signal stays unchanged even after a lapse of t_{LD}, the IC determines this condition as a motor lockup state and activates the motor lock protection (see Section 10.7.5).

The IC can also operate in test mode. In test mode, the high-side transistors in the trapezoidal control are driven at duty cycle = 100%, the TSD circuit is disabled, and the phase advance angle is fixed at 0°. To start IC operations in test mode, turn on the IC after applying a voltage of ≥8.1 V on the VSP pin, and a voltage of 2.75 V (typ.) on the LA pin.

10.3 Charging of Bootstrap Capacitors

It is required to fully charge bootstrap capacitors, C_{Bx}, at startup. The charging sequence depends on the VSP pin voltage, V_{SP}. When 1.0 V ≤ V_{SP} ≤ 2.1 V at startup, the IC turns on the low-side power MOSFETs at every PWM cycle in order to charge C_{Bx}. When V_{SP} ≥ 2.1 V, the IC controls the motor speed according to the VSP pin voltage levels (see Section 10.4). However, note that the IC does not charge C_{Bx} even when 1.0 V ≤ V_{SP} ≤ 2.1 V along with the motor rotating inversely to the preset direction, or the motor coasting at a frequency of ≥1.0 Hz. If a sudden rise in the VSP pin voltage up to 2.1 V or more occurs at startup, the IC starts the motor speed control after charging C_{Bx} for a period of 9 ms ± 5%.

10.4 Motor Speed Control

The IC controls the speed of motor rotation with an analog voltage applied to the VSP pin. When 2.1 V ≤ V_{SP} ≤ 5.4 V, the IC controls its output duty cycles depending on the VSP pin voltage levels. For the IC operation when V_{SP} < 2.1 V (i.e., the startup sequence), see Section 10.2.

A duty cycle of an output signal is determined according to a digital signal that is generated by the built-in 7-bit AD converter from the VSP pin input voltage. The higher the VSP pin voltage increases, the higher the duty cycle becomes, thus causing the motor to rotate faster. Figure 10-13 depicts how a duty cycle varies according to the VSP pin voltage, V_{SP}. While V_{SP} maintains at 5.4 V or more, the IC controls its output signals at duty cycle = 100%.

Figure 10-14 is an internal circuit diagram describing the VSP pin and its peripheral circuit. A voltage to be applied on the VSP pin, V_{SPP}, must be set to <10 V, i.e., below the rated VSP pin input voltage. R_{SP} should have a resistance of about 100 Ω; C_{SP} should have a capacitance of about 0.1 µF.

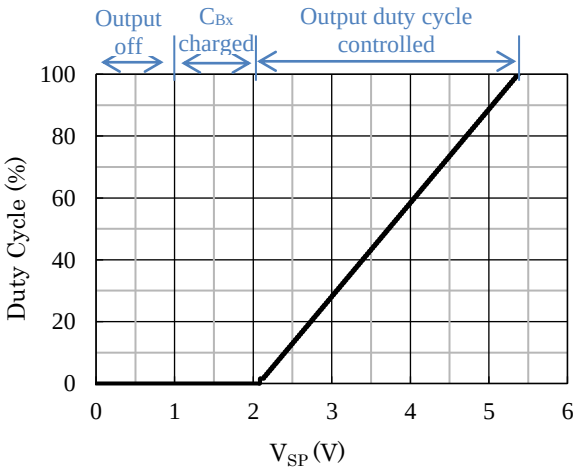

Figure 10-13. VSP Pin Voltage vs. Duty Cycle

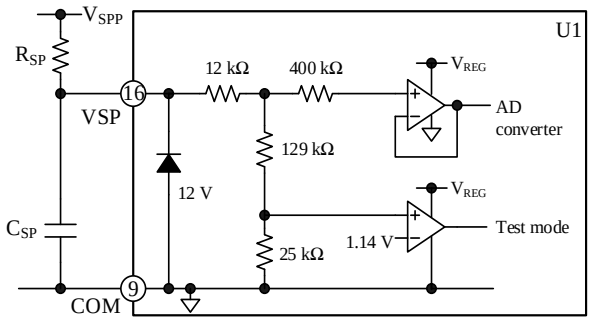

Figure 10-14. Internal Circuit Diagram of VSP Pin and

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Its Peripheral Circuit

10.5 Phase Advance Function

The IC features the phase advance function. The angle of phase advance is determined by an analog voltage applied to the LA pin. As shown in Figure 10-15, the VREG pin voltage divided by two resistors, R_{LA1} and R_{LA2}, is applied to the LA pin. Figure 10-16 plots how a phase advance angle changes over the LA pin voltage. When the phase advance function is enabled, each phase shifts ±0.9375° every 4 cycles of a Hall signal to the preset angle.

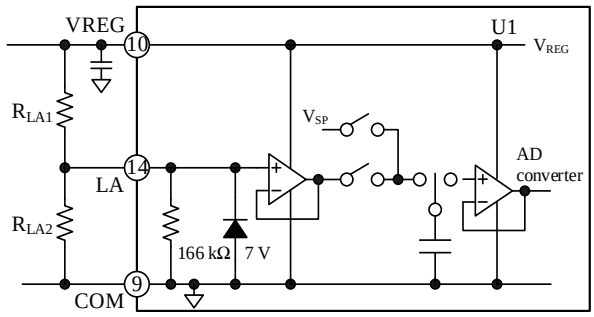

Figure 10-15. Internal Circuit Diagram of LA Pin and Its Peripheral Circuit

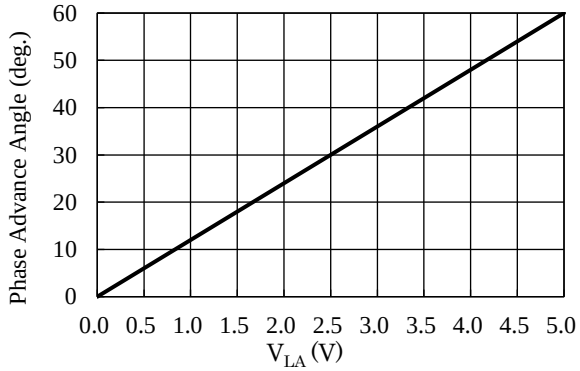

Figure 10-16. LA Pin Voltage vs. Phase Advance Angle

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Table 10-3. Truth Table for Trapezoidal Control (Forward)

Position Sensing Signal			U-phase		V-phase		W-phase	
HU	HV	HW	High-side Transistor	Low-side Transistor	High-side Transistor	Low-side Transistor	High-side Transistor	Low-side Transistor
H	L	H	OFF	ON	ON	OFF	OFF	OFF
H	L	L	OFF	ON	OFF	OFF	ON	OFF
H	H	L	OFF	OFF	OFF	ON	ON	OFF
L	H	L	ON	OFF	OFF	ON	OFF	OFF
L	H	H	ON	OFF	OFF	OFF	OFF	ON
L	L	H	OFF	OFF	ON	OFF	OFF	ON
L	L	L	OFF	OFF	OFF	OFF	OFF	OFF
H	H	H	OFF	OFF	OFF	OFF	OFF	OFF

Table 10-4. Truth Table for Trapezoidal Control (Reverse)

Position Sensing Signal			U-phase		V-phase		W-phase	
HU	HV	HW	High-side Transistor	Low-side Transistor	High-side Transistor	Low-side Transistor	High-side Transistor	Low-side Transistor
L	H	L	OFF	ON	ON	OFF	OFF	OFF
L	H	H	OFF	ON	OFF	OFF	ON	OFF
L	L	H	OFF	OFF	OFF	ON	ON	OFF
H	L	H	ON	OFF	OFF	ON	OFF	OFF
H	L	L	ON	OFF	OFF	OFF	OFF	ON
H	H	L	OFF	OFF	ON	OFF	OFF	ON
H	H	H	OFF	OFF	OFF	OFF	OFF	OFF
L	L	L	OFF	OFF	OFF	OFF	OFF	OFF

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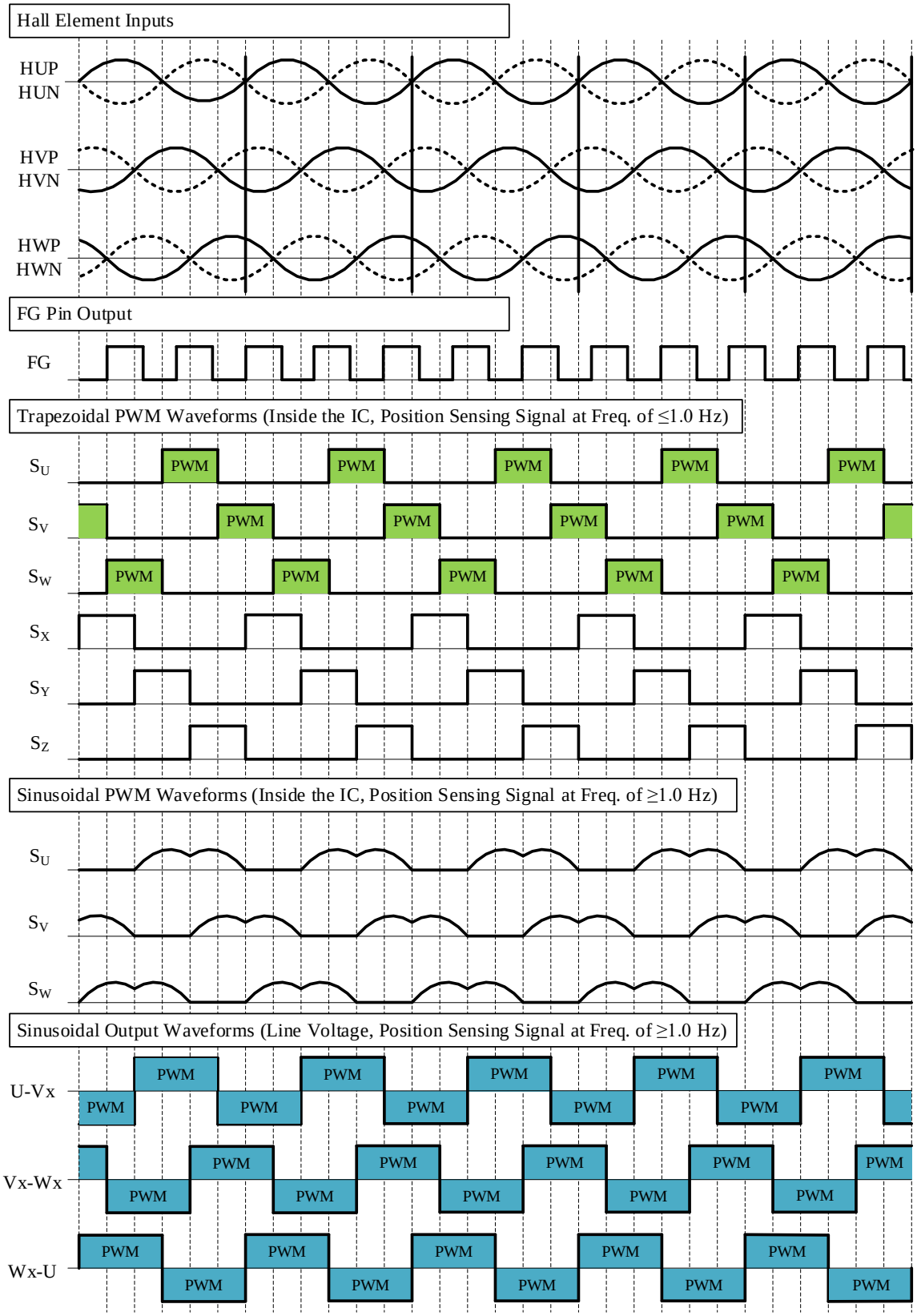

Figure 10-17. Operational Waveforms (Forward, No Phase Advance)

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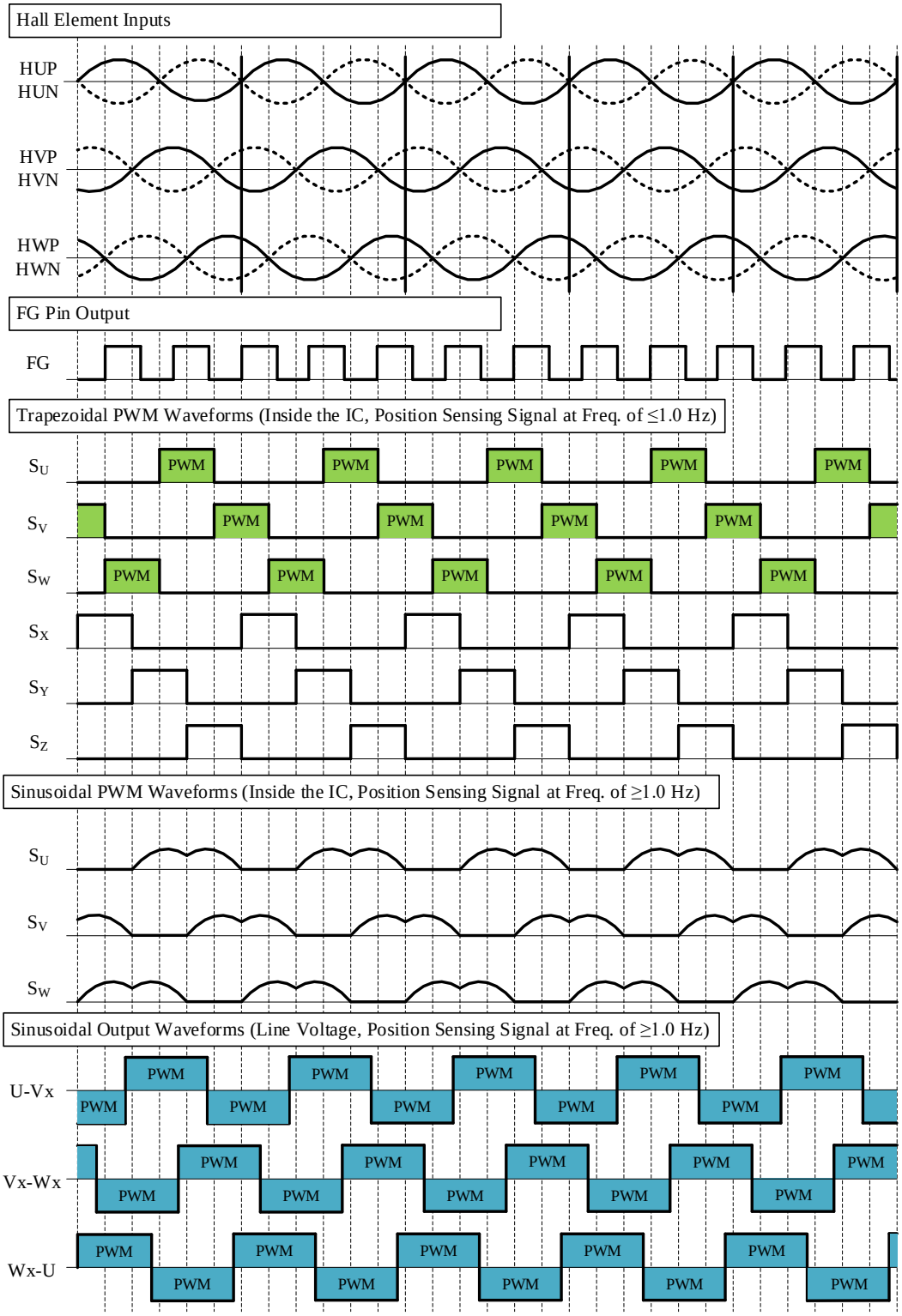

Figure 10-18. Operational Waveforms (Forward, Phase Advance by 15°)

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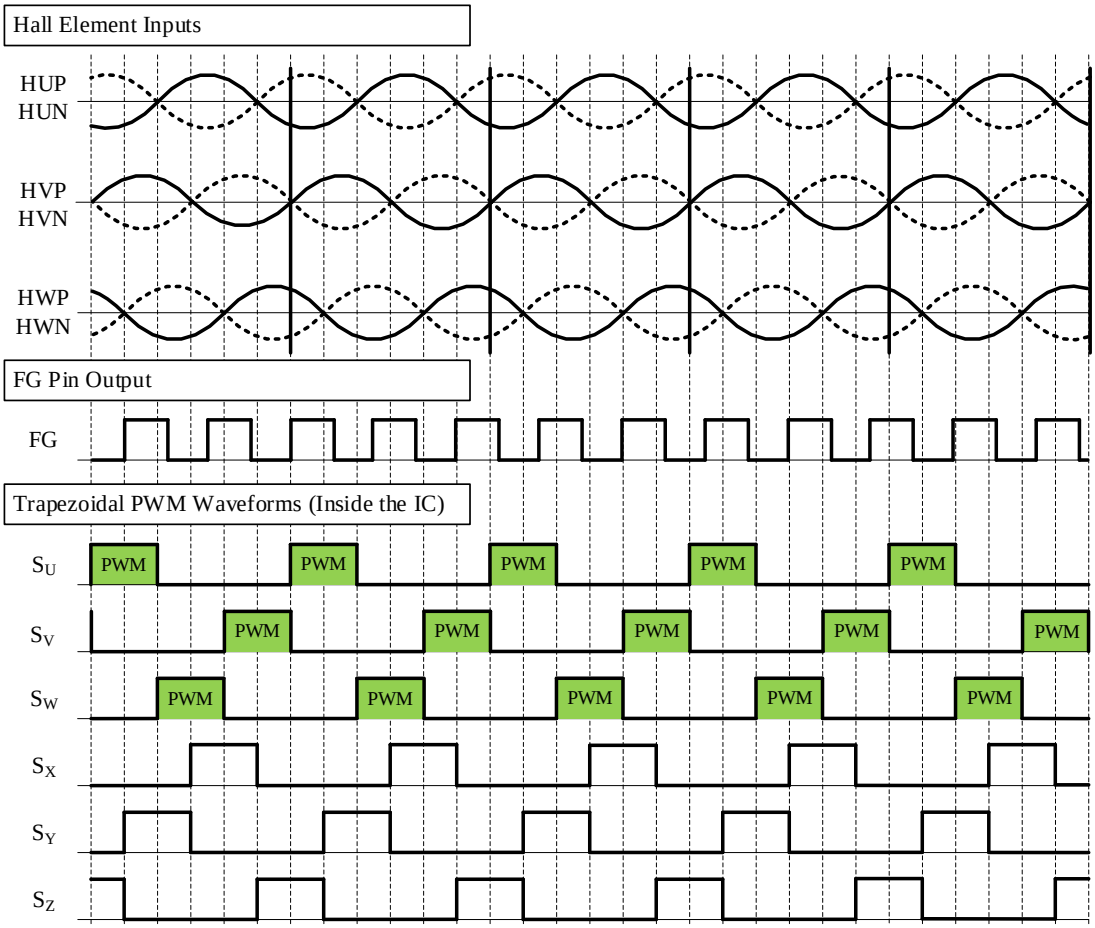

Figure 10-19. Operational Waveforms (Reverse)

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10.6 Fault Signal Output

In case one or more of the following protections are actuated, an internal P-channel power MOSFET turns on, then the FO pin becomes logic high (about 5 V). In normal operation, the FO pin outputs a low signal.

For more details on the protections, see Section 10.7.

- VREG pin undervoltage lockout (UVLO_VREG)
- Overcurrent protection (OCP)
- Thermal shutdown (TSD)
- Motor lock protection (MLP)
- Reverse rotation detection
- Hall signal abnormality detection

The fault signal output time of the FO pin at OCP activation is defined as the OCP Hold Time, t_P, fixed by a built-in feature of the IC itself. t_P = 15 ms when the OSCR pin is open (see Section 10.7.3).

The external microcontroller receives a fault signal with its interrupt pin (INT), and must be programmed to shut off any input signals to the IC within the predetermined OCP hold time, t_P.

10.7 Protection Functions

This section describes the various protection circuits provided in the SX68128MB, such as those designed to detect a voltage drop across power supplies, an overcurrent condition, an abnormal motor state, and so on.

10.7.1 VREG Pin Undervoltage Lockout (UVLO_VREG)

When the VREG pin voltage decreases to V_{UVRL} = 3.6 V or less, the VREG pin undervoltage lockout (UVLO_VREG) circuit gets activated and turns off the high- and low-side power MOSFETs. When the VREG pin voltage increases to V_{UVRH} = 4.0 V or more, the IC releases the UVLO_VREG operation. Then, the high- and low-side power MOSFETs resume operating according to position sensing signals. During the UVLO_VREG operation, the FO pin becomes logic high and transmits fault signals.

10.7.2 Undervoltage Lockout for Power Supplies (UVLO)

In case the gate-driving voltages of the output transistors decrease, their steady-state power dissipations increase. This overheating condition may cause permanent damage to the IC in the worst case. To prevent this event, the SX68128MB has the undervoltage lockout (UVLO) circuits for each of the high-side (the VBx pin) and the low-side (the VCC1 pin) power supplies.

10.7.2.1. VBx Pin (UVLO_VB)

When the voltage between the VBx and output (U, V1/V2, or W1/W2) pins (VBx–HSx) decreases to $V_{BS(OFF)}$ = 10.0 V or less, the UVLO_VB circuit gets activated and turns off the high-side power MOSFETs. When the voltage between the VBx and output pins increases to $V_{BS(ON)}$ = 10.5 V or more, the IC releases the UVLO_VB operation. Then, the high-side power MOSFETs resume operating according to position sensing signals.

10.7.2.2. VCC1 Pin (UVLO_VCC)

When the VCC1 pin voltage decreases to $V_{CC(OFF)}$ = 11.0 V or less, the UVLO_VCC circuit gets activated and turns off the high- and low-side power MOSFETs. When the VCC1 pin voltage increases to $V_{CC(ON)}$ = 11.5 V or more, the IC releases the UVLO_VCC operation. Then, the high- and low-side power MOSFETs resume operating according to position sensing signals.

10.7.3 Overcurrent Limit (OCL) and Overcurrent Protection (OCP)

The IC has two different protections against overcurrent conditions: the overcurrent limit (OCL) and the overcurrent protection (OCP).

Figure 10-20 is an internal circuit diagram describing the OCP pin and its peripheral circuit. The OCP pin detects overcurrents with voltage across an external shunt resistor, R_S. Because the OCP pin is internally pulled up, the OCP pin voltage increases proportionally to a rise in the current running through the shunt resistor, R_S.

Note that overcurrents are undetectable when one or more of the U, V1/V2, and W1/W2 pins or their traces are shorted to ground (ground fault). In case any of these pins falls into a state of ground fault, the output transistors may be destroyed.

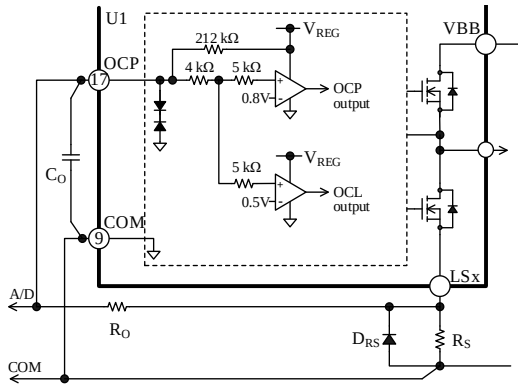

Figure 10-20. Internal Circuit Diagram of OCP Pin and Its Peripheral Circuit

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The overcurrent limit (OCL) is a protection against relatively low overcurrent conditions. When the OCP pin voltage increases to V_{LIM} = 0.50 V or more, and remains in this condition for a period of a blanking time ($t_{BK(OCL)}$ = 1.9 µs when OSCR = open) or longer, the IC turns off the high- and low-side power MOSFETs. The OCL operation is automatically released at each PWM cycle.

The overcurrent protection (OCP) is a protection against large inrush currents. When the OCP pin voltage increases to V_{TRIP} = 0.8 V or more, and remains in this condition for a period of a blanking time ($t_{BK(OCP)}$ = 1.3 µs when OSCR = open) or longer, the OCP circuit is activated. Then, the high- and low-side power MOSFETs are turned off for a certain period of time (t_P = 15 ms when OSCR = open). After that, the high- and low-side power MOSFETs resume operating according to position sensing signals. During the OCP operation, the FO pin goes logic high and sends fault signals.

The OCL and OCP are used for detecting abnormal conditions, such as an output transistor shorted. In case short-circuit conditions occur repeatedly, the output transistors can be destroyed. For this reason, motor operations must be controlled by the external microcontroller so that it can immediately stop the motor when fault signals are detected. If you need to resume the IC operation thereafter, set the IC to be resumed after a lapse of ≥2 seconds.

For proper shunt resistor setting, your application must meet the following:

- Use the shunt resistor that has a recommended resistance, R_S (see Section 2).
- Set the OCP pin input voltage to vary within the rated input voltages, $V_{IN(2)}$ (see Section 1).
- Keep the current through the output transistors below the rated output current (pulse), I_{OP} (see Section 1).

It is required to use a resistor with low internal inductance because high-frequency switching current will flow through the shunt resistors, R_S. In addition, choose a resistor with allowable power dissipation according to your application.

10.7.4 Thermal Shutdown (TSD)

The SX68128MB incorporates the thermal shutdown (TSD) circuit. In case of overheating (e.g., increased power dissipation due to overload, or elevated ambient temperature at the device), the IC shuts down the high- and low-side power MOSFETs.

The TSD circuit in the MIC for gate driver monitors temperatures (see Figure 5-1). When the junction temperature of the MIC for gate driver, $T_{J(DRV)}$, exceeds T_{DH} = 130 °C, the TSD circuit is activated. When $T_{J(DRV)}$ decreases to T_{DL} = 90 °C or less, the shutdown condition is released. The output transistors then resume operating according to input signals. During the TSD operation, the FO pin becomes logic high and transmits fault signals. Note that junction temperatures of the output transistors themselves are not monitored; therefore, do not use the TSD function as an overtemperature prevention for the output transistors.

10.7.5 Motor Lock Protection (MLP)

When the state in which a position sensing signal stays unchanged within a rotation of 60° electrical angle persists for a motor lock hold time (t_{LD} = 6 s when OSCR = open) or longer, the motor lock protection (MLP) circuit gets activated.

Then, the high- and low-side power MOSFETs are turned off for a certain period of time (t_{LH} = 35 s when OSCR = open). After that, the high- and low-side power MOSFETs resume operating according to position sensing signals.

During the MLP operation, the FO pin becomes logic high and transmits fault signals. Moreover, direct currents through the power MOSFETs cause an increase in the junction temperatures of the power MOSFETs. Therefore, care must be taken not to allow the junction temperatures to exceed the absolute maximum rating.

10.7.6 Reverse Rotation Detection

In case the motor rotates in a direction opposite to the preset direction, the reverse rotation detection function gets activated and puts the FO pin into a high state (i.e., a fault signal output). When the motor rotates in the preset direction, the FO pin is in a low state. When the IC detects a reverse rotation state during motor rotations, the motor driving system is immediately switched to the trapezoidal control before a rotation of 60° electrical angle completes.

Table 10-5. Motor Driving Controls during Reverse Rotation

CW/CCW Pin State	Motor Direction	Driving System
L (Reverse)	Forward	Trapezoidal
	Reverse	Sinusoidal
H (Forward)	Forward	Sinusoidal
	Reverse	Trapezoidal

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10.7.7 Hall Signal Abnormality Detection

As Figure 10-21 shows, signals from the external Hall elements are input into the corresponding comparators. The IC then receives the comparator outputs as the motor positional information, i.e., position sensing signals.

When all the position sensing signals (HU, HV, HW) are either in a high or low state, the Hall signal abnormality detection function gets activated and turns off the high- and low-side power MOSFETs. When the IC detects input states other than those above, each of the high- and low-side power MOSFETs responds in accordance with the input logic levels of the position sensing signals. For the truth tables for the position sensing signals and the output transistors, see Table 10-3 and Table 10-4. While the function is being enabled, the FO pin becomes logic high and sends fault signals.

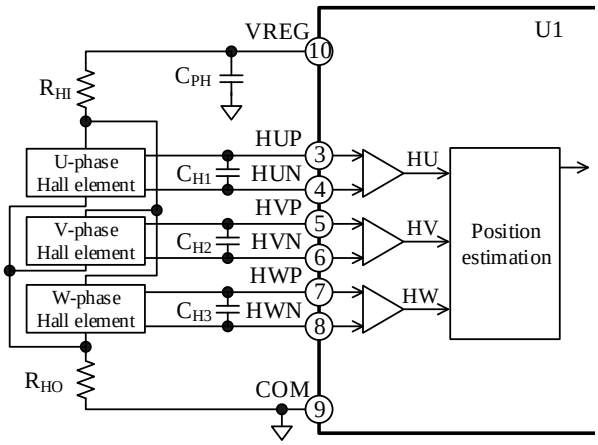

Figure 10-21. Internal Circuit Diagram of HxP and HxN Pins and Their Peripheral Circuit

11. Design Notes

11.1 PCB Pattern Layout

Figure 11-1 shows a schematic diagram of a motor drive circuit. The circuit consists of current paths having high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing.

Current loops, which have high frequencies and high voltages, should be as small and wide as possible, in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

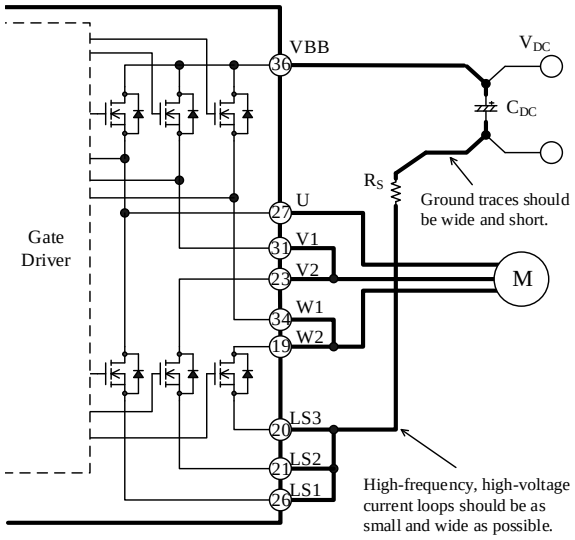

Figure 11-1. High-frequency, High-voltage Current Paths

11.2 Considerations in IC Characteristics Measurement

When measuring the leakage current of the output transistors (power MOSFETs) incorporated in the IC, note that all of the output (U, V1, V2, W1, W2), LSx, and COM pins must be appropriately connected. Otherwise, the output transistors may result in permanent damage. Also note that the gate and source of each output transistor should have the same potential during the leakage current measurement. Moreover, care should be taken during the measurement because each output transistor is connected as follows:

- All the high-side drains are internally connected to the VBB pin.
- In the U-phase, the high-side source and the low-side drain are internally connected to the U pin. (In the V- and W-phases, the high- and low-side transistors are unconnected inside the IC.)
- The high-side gates are internally pulled down to the output pins.
- The low-side gates are internally pulled down to the COM pin.

The following are circuit diagrams representing typical measurement circuits for leakage current: Figure 11-2 shows the high-side transistor (Q_{1H}) in the U-phase; Figure 11-3 shows the low-side transistor (Q_{1L}) in the U-phase. And all the pins that are not represented in these figures are open. When measuring the high-side transistors, leave all the non-measuring pins open. When measuring the low-side transistors, connect only the measuring LSx pin to the COM pin and leave the other pins open.

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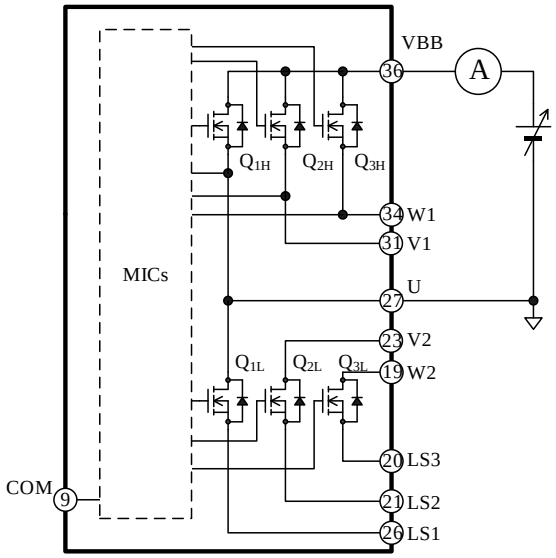

Figure 11-2. Typical Measurement Circuit for High-side Transistor (Q_{1H}) in U-phase

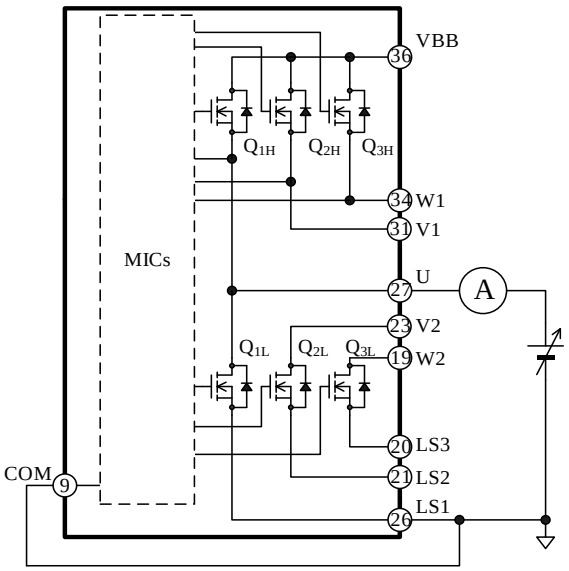

Figure 11-3. Typical Measurement Circuit for Low-side Transistor (Q_{1L}) in U-phase

12. Calculating Power Losses and Estimating Junction Temperature

This section describes the procedures to calculate power losses in output transistors (power MOSFETs), and to estimate a junction temperature. Note that the descriptions listed here are applicable to the IC, which is controlled by a 3-phase sine-wave PWM driving strategy. For quick and easy references, we offer calculation support tools online. Please visit our website to find out more.

- DT0050: SX68128MB Calculation Tool
  https://www.semicon.sanken-ele.co.jp/en/calc-tool/mosfet_caltool_en.html

Total power loss in a power MOSFET can be obtained by taking the sum of the following losses: steady-state loss, P_{RON}; switching loss, P_{SW}; the steady-state loss of a body diode, P_{SD}. In the calculation procedure we offer, the recovery loss of a body diode, P_{RR}, is considered negligibly small compared with the ratios of other losses.

The following subsections contain the mathematical procedures to calculate these losses (P_{RON}, P_{SW}, and P_{SD}) and the junction temperature of all power MOSFETs operating.

12.1 Power MOSFET Steady-state Loss, P_{RON}

Steady-state loss in a power MOSFET can be computed by using the $R_{DS(ON)}$ vs. I_D curves, listed in Section 13.3.1. As expressed by the curves in Figure 12-1, a linear approximation at a range the I_D is actually used is obtained by: $R_{DS(ON)} = \alpha \times I_D + \beta$.

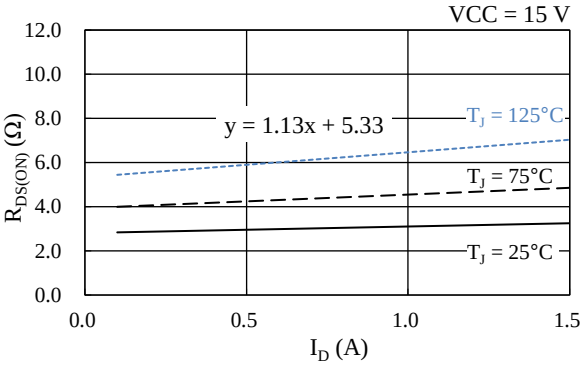

Figure 12-1. Linear Approximate Equation of $R_{DS(ON)}$ vs. I_D Curve

The values gained by the above calculation are then applied as parameters in Equation (4), below. Hence, the equation to obtain the power MOSFET steady-state loss, P_{RON}, is:

$$P_{RON} = \frac{1}{2\pi}\int_0^{\pi} I_D(\varphi)^2 \times R_{DS(ON)}(\varphi) \times DT \times d\varphi$$

$$= 2\sqrt{2}\alpha\left(\frac{1}{3\pi} + \frac{3}{32}M \times \cos\theta\right) {I_M}^3 + 2\beta\left(\frac{1}{8} + \frac{1}{3\pi}M \times \cos\theta\right) {I_M}^2 . \quad (4)$$

Where:

I_D is the drain current of the power MOSFET (A),

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$R_{DS(ON)}$ is the drain-to-source on-resistance of the power MOSFET (Ω),
DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),
cosθ is the motor power factor (0 to 1),
I_M is the effective motor current (A),
α is the slope of the linear approximation in the $R_{DS(ON)}$ vs. I_D curve, and
β is the intercept of the linear approximation in the $R_{DS(ON)}$ vs. I_D curve.

12.2 Power MOSFET Switching Loss, P_{SW}

Switching loss in a power MOSFET can be calculated by Equation (5), letting I_M be the effective current value of the motor:

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{300}. \quad (5)$$

Where:
f_C is the PWM carrier frequency (Hz),
V_{DC} is the main power supply voltage (V), i.e., the VBB pin input voltage, and
α_E is the slope on the switching loss curve (see Section 13.3.2).

12.3 Body Diode Steady-state Loss, P_{SD}

Steady-state loss in the body diode of a power MOSFET can be computed by using the V_{SD} vs. I_{SD} curves, listed in Section 13.3.1. As expressed by the curves in Figure 12-2, a linear approximation at a range the I_{SD} is actually used is obtained by: $V_{SD} = \alpha \times I_{SD} + \beta$.

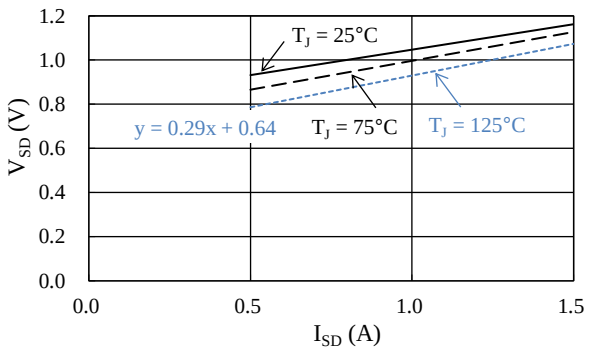

Figure 12-2. Linear Approximate Equation of V_{SD} vs. I_{SD} Curve

The values gained by the above calculation are then applied as parameters in Equation (6), below. Hence, the equation to obtain the body diode steady-state loss, P_{SD}, is:

$$P_{SD} = \frac{1}{2\pi}\int_0^{\pi} V_{SD}(\varphi) \times I_{SD}(\varphi) \times (1 - DT) \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2} - \frac{4}{3\pi}M \times \cos\theta\right) {I_M}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2} - \frac{\pi}{8}M \times \cos\theta\right) I_M. \quad (6)$$

Where:
V_{SD} is the source-to-drain diode forward voltage of the power MOSFET (V),
I_{SD} is the source-to-drain diode forward current of the power MOSFET (A),
DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),
cosθ is the motor power factor (0 to 1),
I_M is the effective motor current (A),
α is the slope of the linear approximation in the V_{SD} vs. I_{SD} curve, and
β is the intercept of the linear approximation in the V_{SD} vs. I_{SD} curve.

12.4 Estimating Junction Temperature of Power MOSFET

The junction temperature of all power MOSFETs operating, T_J, can be estimated with Equation (7):

$$T_J = R_{J-C} \times \{(P_{RON} + P_{SW} + P_{SD}) \times 6\} + T_C. \quad (7)$$

Where:
R_{J-C} is the junction-to-case thermal resistance (°C/W) of all the power MOSFETs operating, and
T_C is the case temperature (°C), measured at the point defined in Figure 3-2.

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13. Performance Curves

13.1 Transient Thermal Resistance Curves

The following graph represents transient thermal resistance (the ratios of transient thermal resistance), with steady-state thermal resistance = 1.

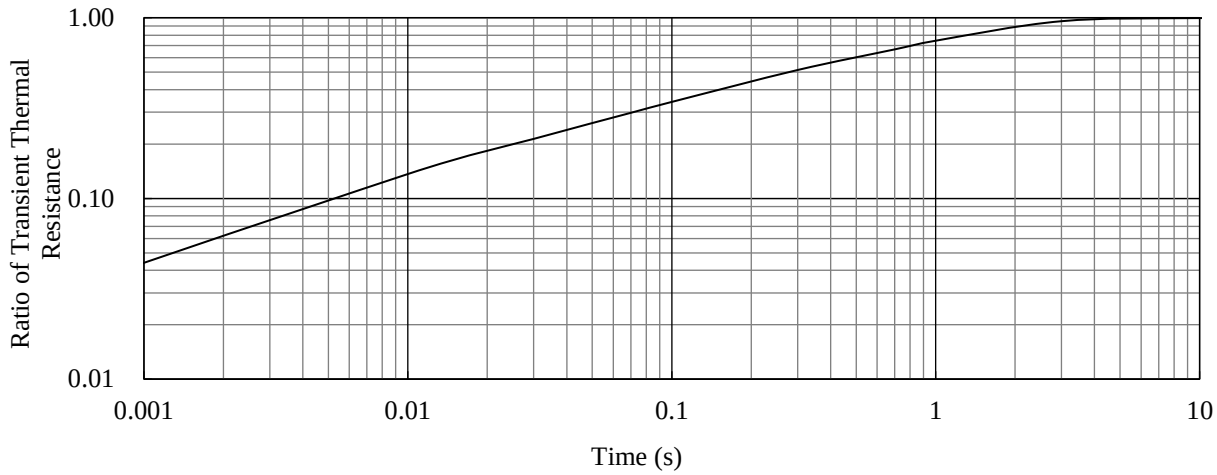

Figure 13-1. Transient Thermal Resistance

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13.2 Performance Curves of Control Parts

Figure 13-4 to Figure 13-22 provide performance curves of the control parts integrated in the SX68128MB, including variety-dependent characteristics and thermal characteristics. T_J represents the junction temperature of the control parts.

Table 13-1. Typical Characteristics of Control Parts

Figure Number	Figure Caption
Figure 13-2	Logic Supply Current in 1-phase Operation (V_{SP} = 0 V), I_{BS} vs. T_C
Figure 13-3	Logic Supply Current in 1-phase Operation (V_{SP} = 5.4 V), I_{BS} vs. T_C
Figure 13-4	Logic Supply Current, I_{CC} vs. T_C
Figure 13-5	Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C
Figure 13-6	Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C
Figure 13-7	Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C
Figure 13-8	Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C
Figure 13-9	MLP Pin High Level Input Current, I_{IH1_MLP} vs. T_C
Figure 13-10	CW/CCW Pin High Level Input Current, $I_{IH1\_CW/CCW}$ vs. T_C
Figure 13-11	LA Pin High Level Input Current, I_{IH1_LA} vs. T_C
Figure 13-12	VSP Pin High Level Input Current, I_{IH1_VSP} vs. T_C
Figure 13-13	OCP Pin High Level Input Current, I_{IH2_OCP} vs. T_C
Figure 13-14	FG Pin High Level Output Voltage, V_{OH} vs. T_C
Figure 13-15	FO Pin High Level Output Voltage, $V_{FO(H)}$ vs. T_C
Figure 13-16	High Level Threshold Voltage (MLP or CW/CCW Pin), V_{IH} vs. T_C
Figure 13-17	Low Level Output Voltage (MLP or CW/CCW Pin), V_{IL} vs. T_C
Figure 13-18	UVLO_VB Filtering Time vs. T_C
Figure 13-19	UVLO_VCC Filtering Time vs. T_C
Figure 13-20	Current Limit Reference Voltage, V_{LIM} vs. T_C
Figure 13-21	OCP Threshold Voltage, V_{TRIP} vs. T_C
Figure 13-22	OCL Blanking Time, $t_{BK(OCL)}$ + Propagation Delay, t_D vs. T_C
Figure 13-23	OCP Blanking Time, $t_{BK(OCP)}$ + Propagation Delay, t_D vs. T_C
Figure 13-24	OCP Hold Time, t_P vs. T_C
Figure 13-25	VREG Pin Voltage, V_{REG} vs. T_C

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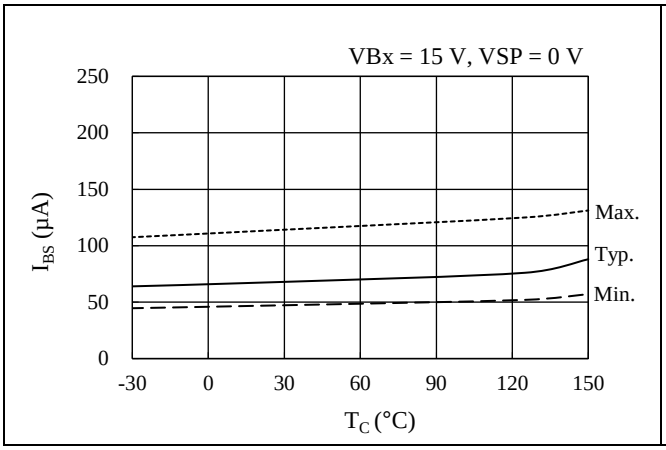

Figure 13-2. Logic Supply Current in 1-phase Operation (V_{SP} = 0 V), I_{BS} vs. T_C

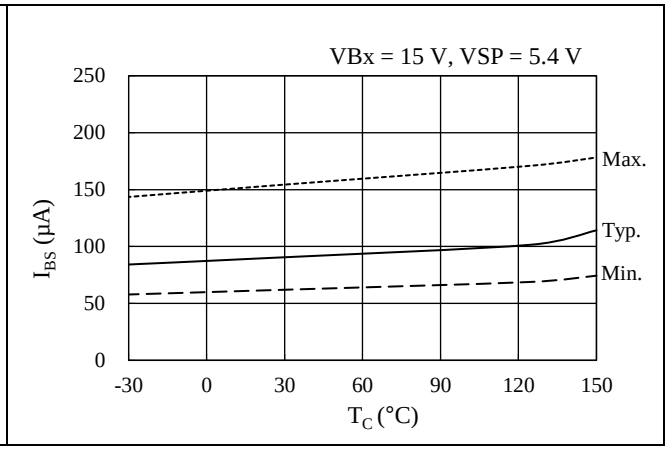

Figure 13-3. Logic Supply Current in 1-phase Operation (V_{SP} = 5.4 V), I_{BS} vs. T_C

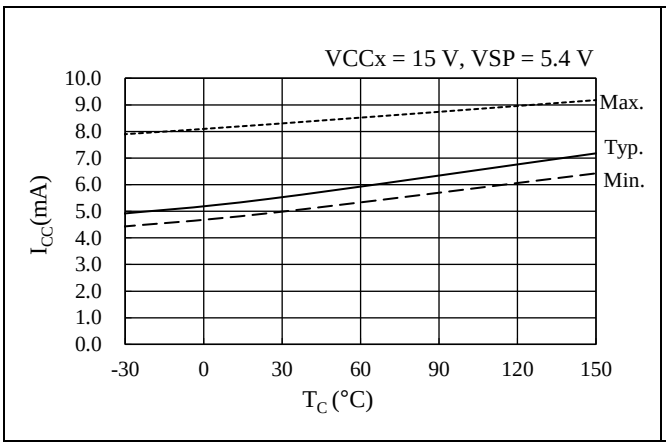

Figure 13-4. Logic Supply Current, I_{CC} vs. T_C

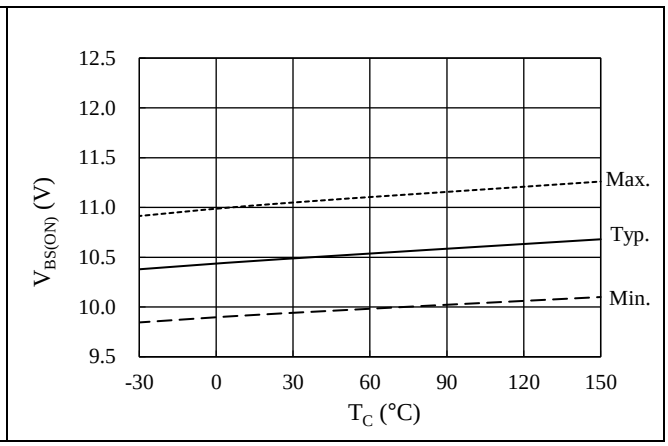

Figure 13-5. Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C

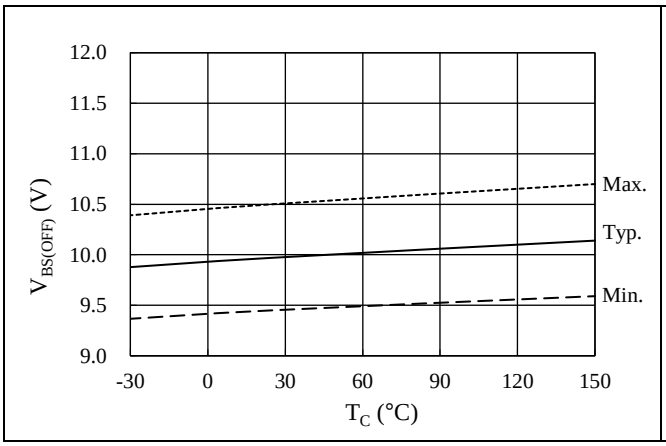

Figure 13-6. Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C

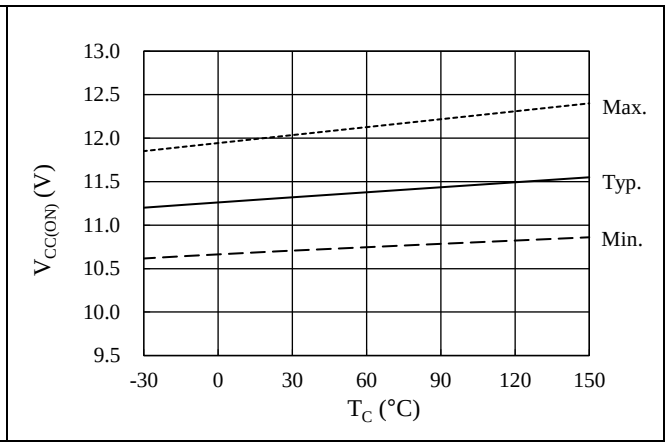

Figure 13-7. Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C

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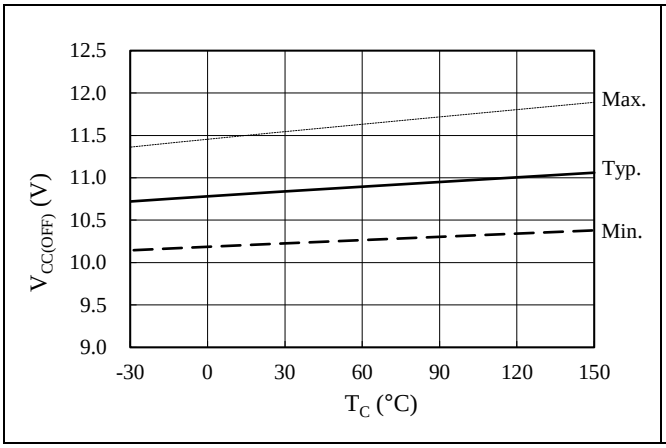

Figure 13-8. Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C

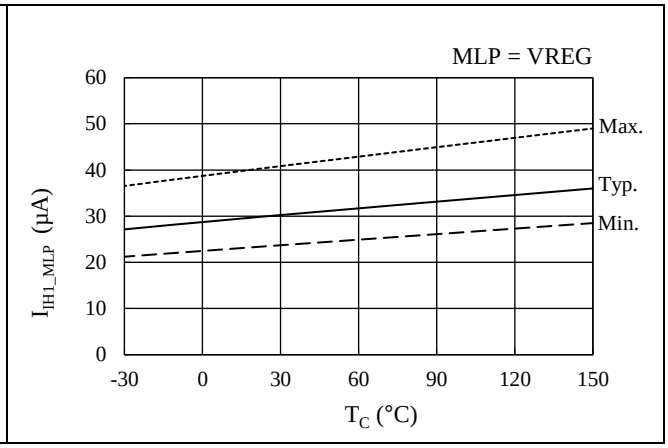

Figure 13-9. MLP Pin High Level Input Current, I_{IH1_MLP} vs. T_C

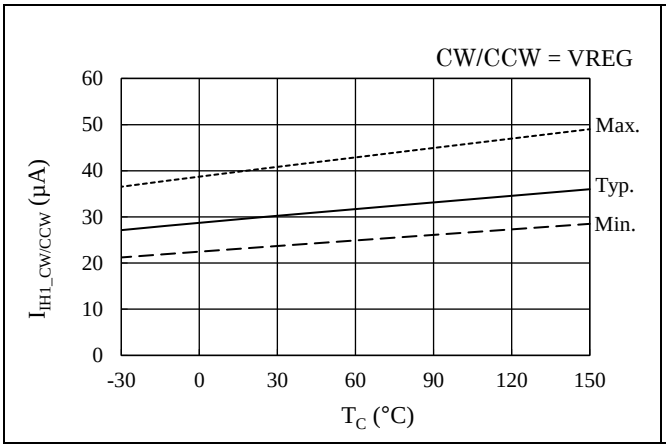

Figure 13-10. CW/CCW Pin High Level Input Current, $I_{IH1\_CW/CCW}$ vs. T_C

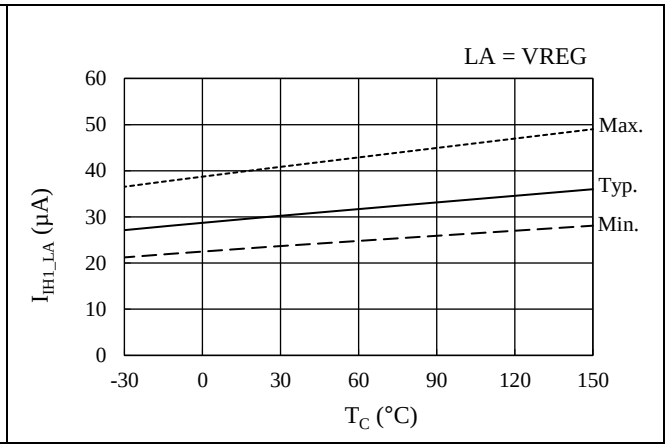

Figure 13-11. LA Pin High Level Input Current, I_{IH1_LA} vs. T_C

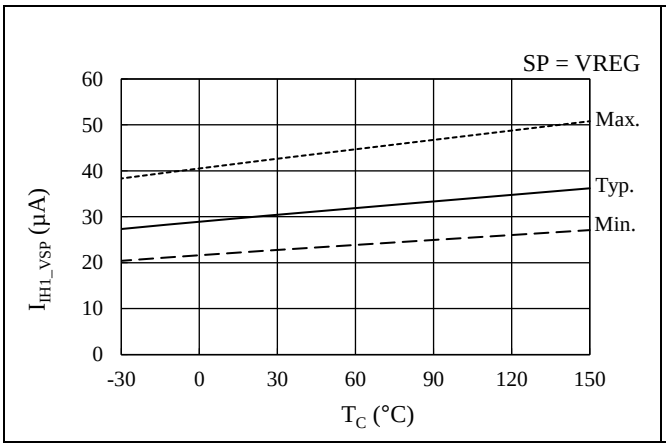

Figure 13-12. VSP Pin High Level Input Current, I_{IH1_VSP} vs. T_C

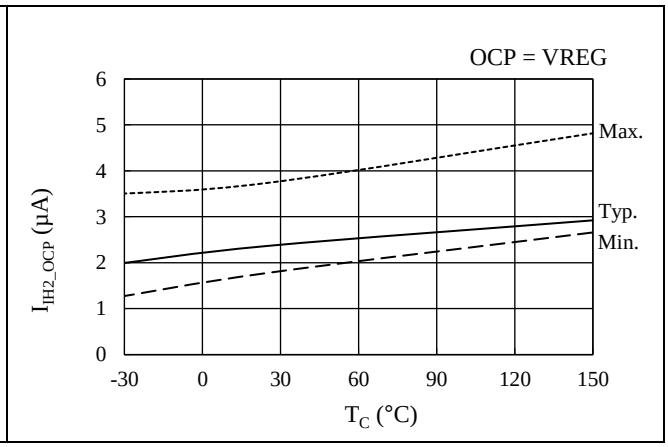

Figure 13-13. OCP Pin High Level Input Current, I_{IH2_OCP} vs. T_C

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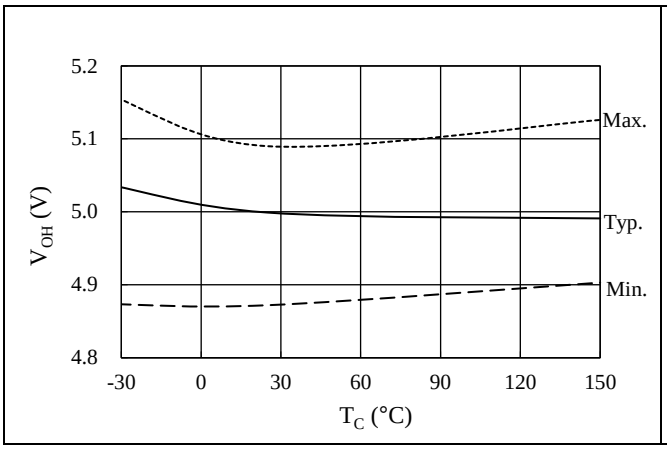

Figure 13-14. FG Pin High Level Output Voltage, V_{OH} vs. T_C

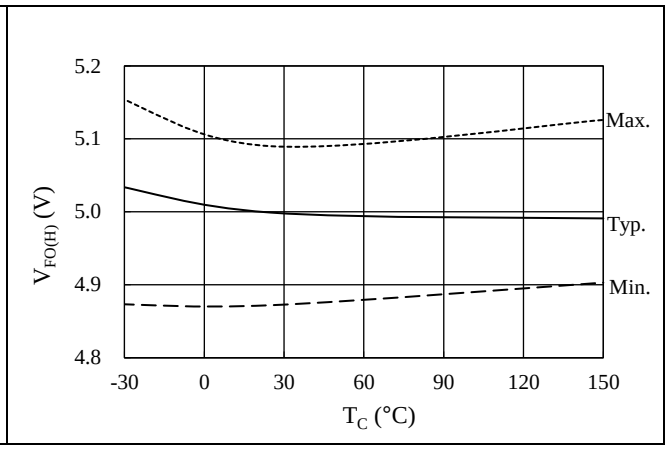

Figure 13-15. FO Pin High Level Output Voltage, $V_{FO(H)}$ vs. T_C

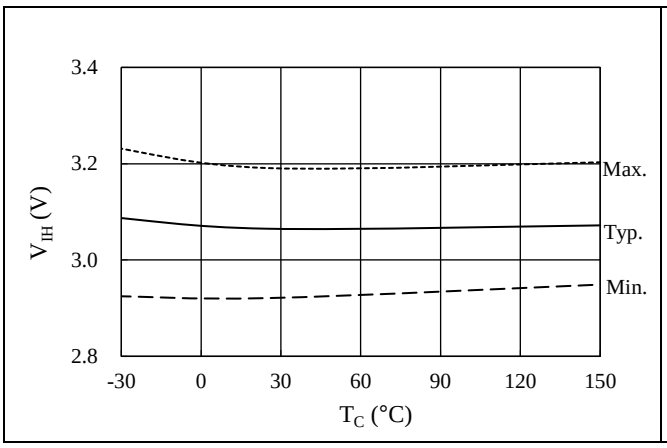

Figure 13-16. High Level Threshold Voltage (MLP or CW/CCW Pin), V_{IH} vs. T_C

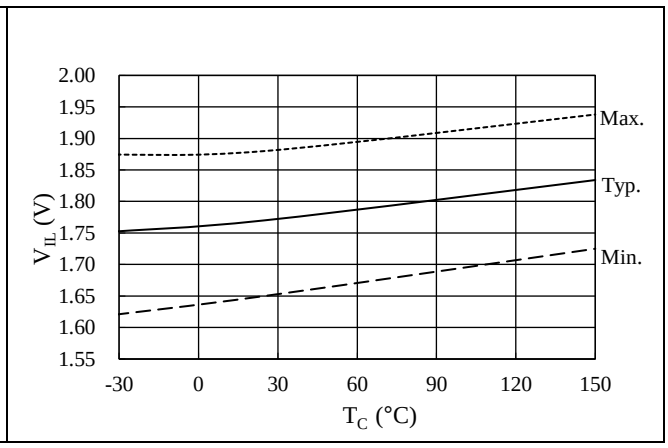

Figure 13-17. Low Level Threshold Voltage (MLP or CW/CCW Pin), V_{IL} vs. T_C

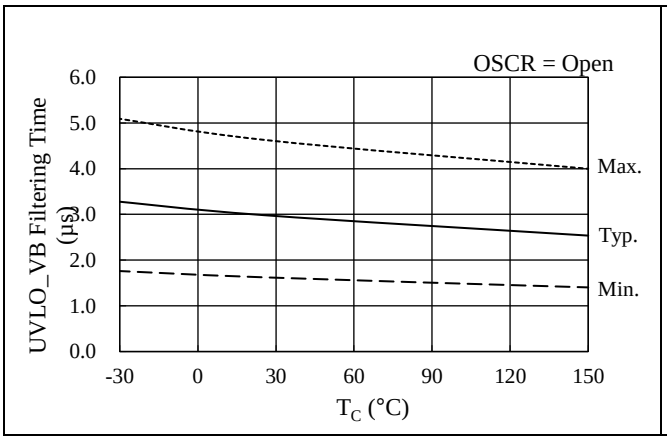

Figure 13-18. UVLO_VB Filtering Time vs. T_C

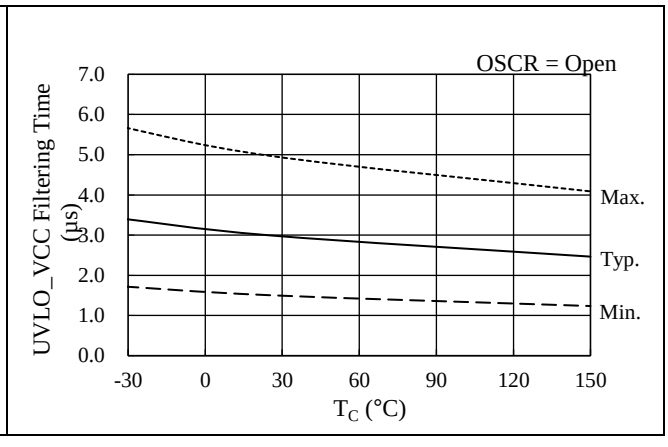

Figure 13-19. UVLO_VCC Filtering Time vs. T_C

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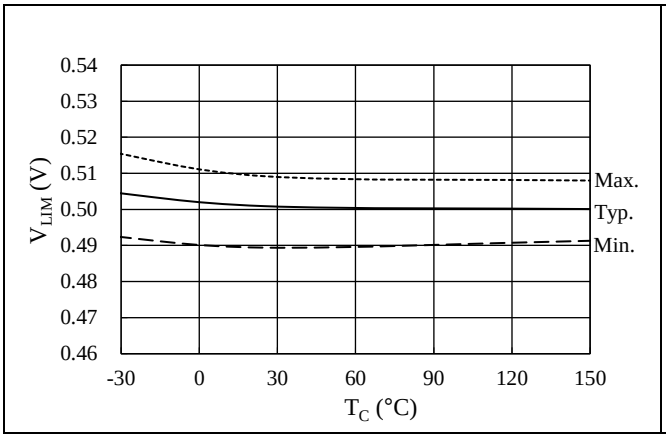

Figure 13-20. Current Limit Reference Voltage, V_{LIM} vs. T_C

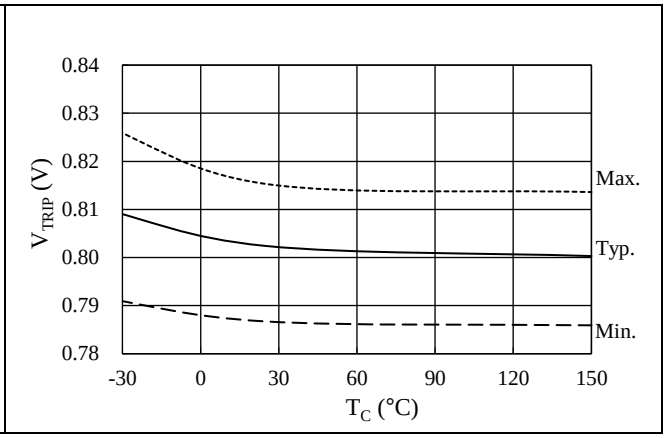

Figure 13-21. OCP Threshold Voltage, V_{TRIP} vs. T_C

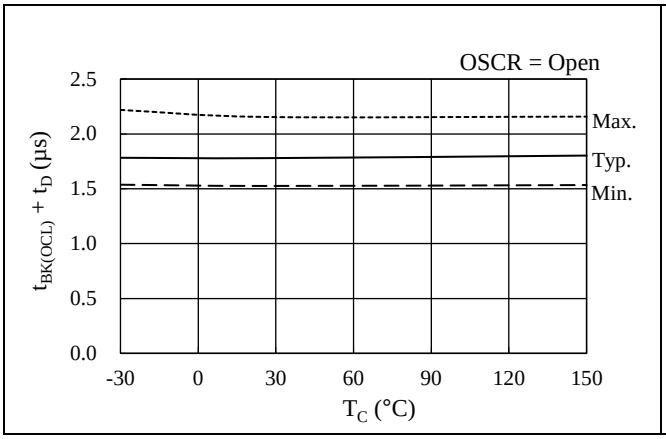

Figure 13-22. OCL Blanking Time, $t_{BK(OCL)}$ + Propagation Delay, t_D vs. T_C

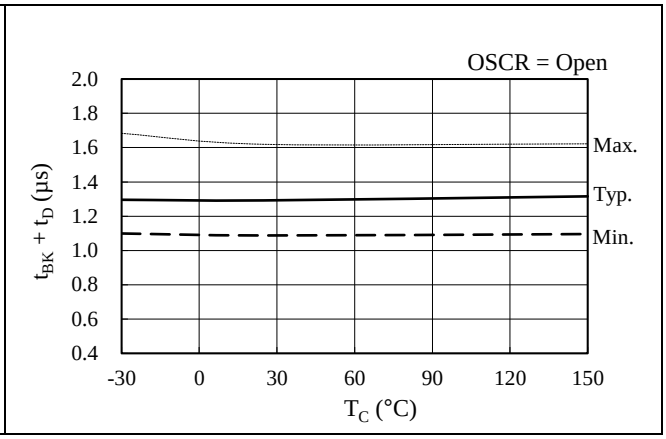

Figure 13-23. OCP Blanking Time, $t_{BK(OCP)}$ + Propagation Delay, t_D vs. T_C

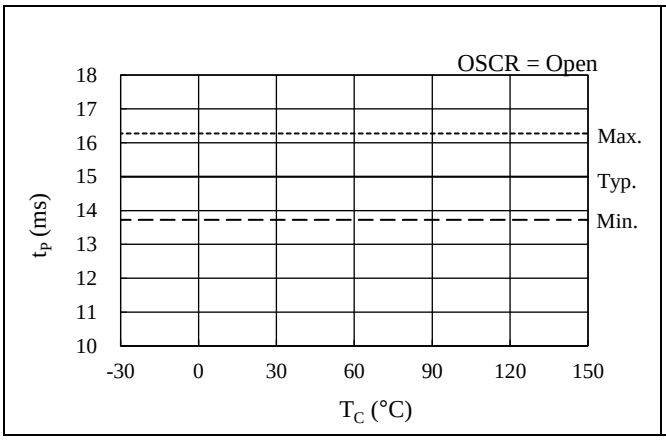

Figure 13-24. OCP Hold Time, t_P vs. T_C

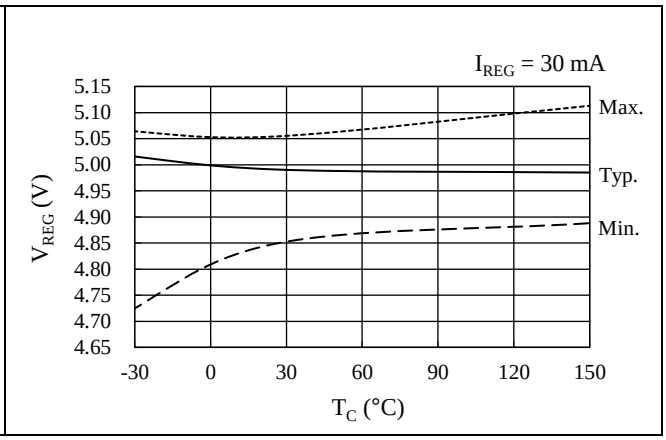

Figure 13-25. VREG Pin Voltage, V_{REG} vs. T_C

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13.3 Performance Curves of Output Parts

13.3.1 Output Transistor Performance Curves

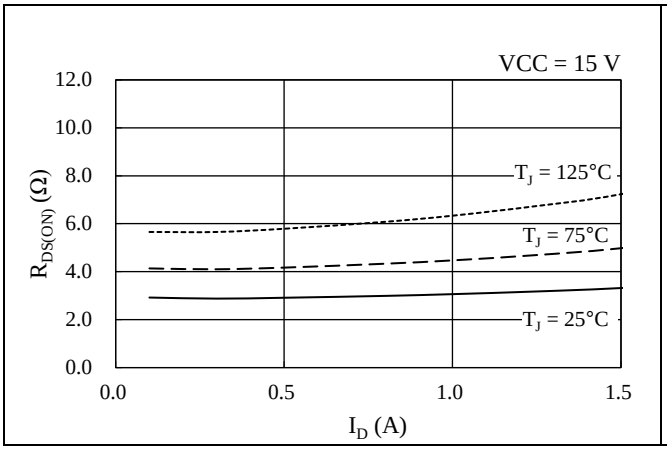

Figure 13-26. Power MOSFET $R_{DS(ON)}$ vs. I_D

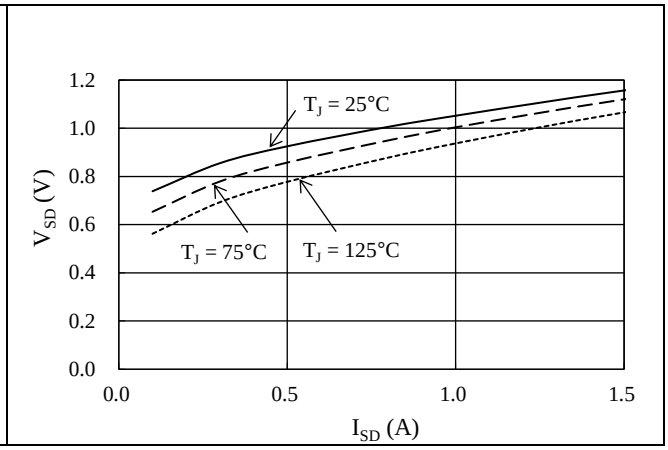

Figure 13-27. Power MOSFET V_{SD} vs. I_{SD}

13.3.2 Switching Loss Curves

Conditions: VBB pin voltage = 300 V, half-bridge circuit with inductive load.
Switching Loss, E, is the sum of turn-on loss and turn-off loss.

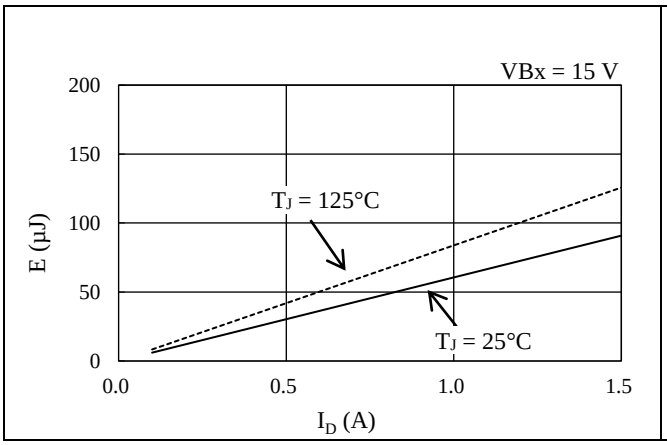

Figure 13-28. High-side Switching Loss

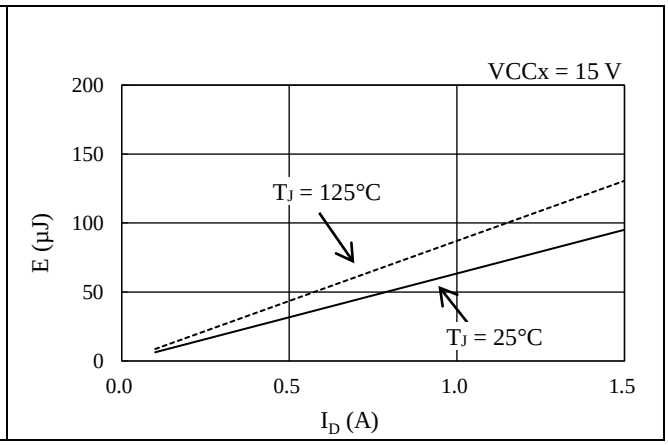

Figure 13-29. Low-side Switching Loss

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13.4 Allowable Effective Current Curves

The following curves represent allowable effective currents in 3-phase sine-wave PWM driving with parameters such as typical $R_{DS(ON)}$ or $V_{CE(SAT)}$, and typical switching losses.

Operating conditions: VBB pin input voltage, V_{DC} = 300 V; VCCx pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_J = 150 °C.

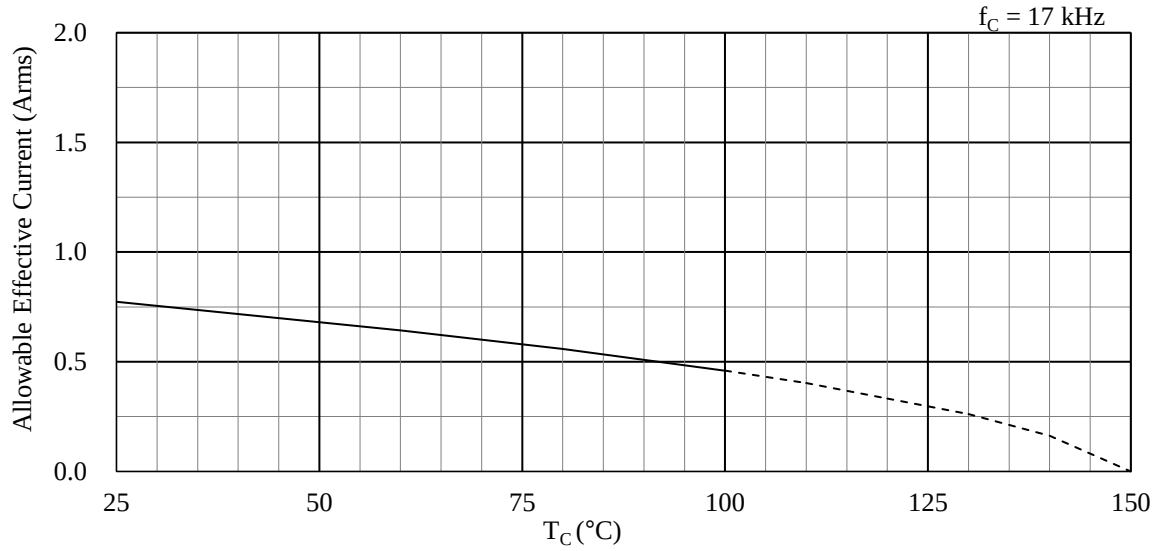

Figure 13-30. Allowable Effective Current (f_C = 17 kHz)

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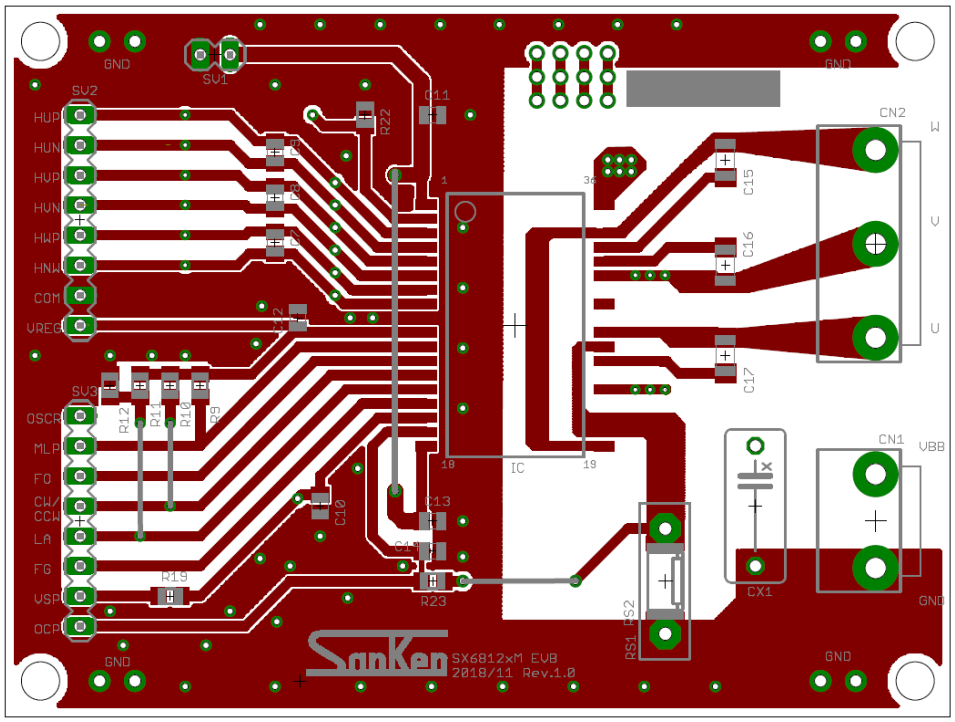
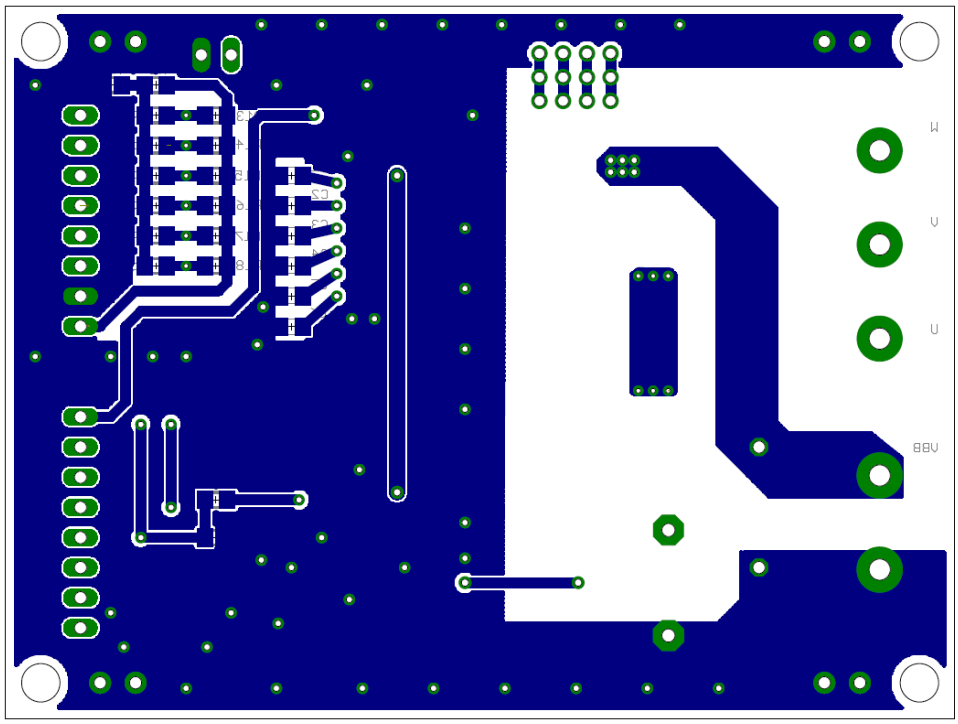
14. Pattern Layout Example

This section contains the schematic diagrams of a PCB pattern layout example using an SX68128MB device. For details on the land pattern example of the IC, see Section 8.



(Top View)



(Bottom View)

Figure 14-1. Pattern Layout Example

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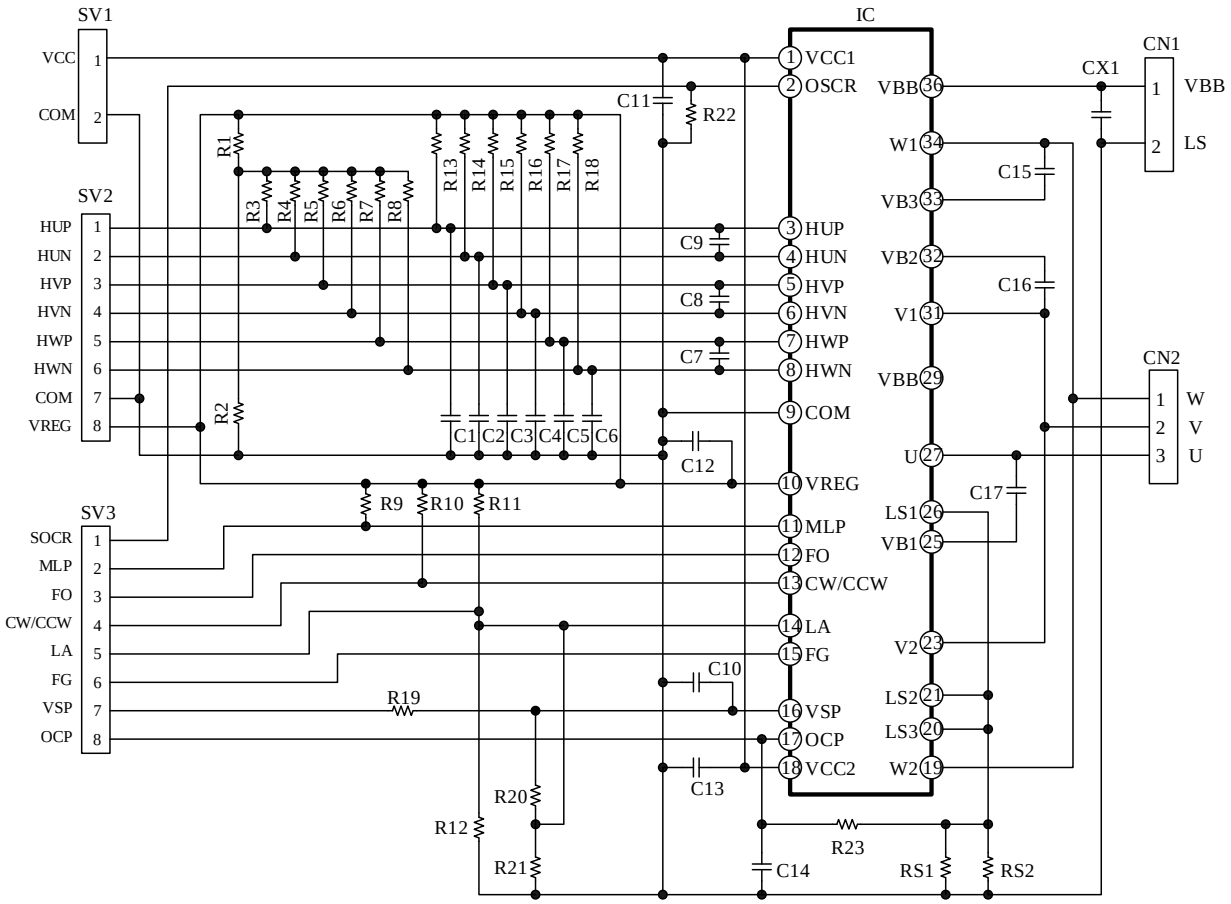

Figure 14-2. Circuit Diagram of PCB Pattern Layout Example

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15. Typical Motor Driver Application

This section contains the information on the typical motor driver application listed in the previous section, including a circuit diagram, specifications, and the bill of the materials used.

- **Motor Driver Specifications**

IC	SX68128MB
Main Supply Voltage, V_{DC}	300 VDC (typ.)
Rated Output Power	50 W

- **Circuit Diagram**

See Figure 14-2.

- **Bill of Materials**

Symbol	Part Type	Ratings	Symbol	Part Type	Ratings
C1	Ceramic	0.1 µF, 35 V	R9(1)	General	Open
C2	Ceramic	0.1 µF, 35 V	R10(2)	General	0 Ω, 1/8 W
C3	Ceramic	0.1 µF, 35 V	R11	General	Open
C4	Ceramic	0.1 µF, 35 V	R12	General	Open
C5	Ceramic	0.1 µF, 35 V	R13(3)	General	Open
C6	Ceramic	0.1 µF, 35 V	R14(3)	General	Open
C7	Ceramic	0.01 µF, 35 V	R15(3)	General	Open
C8	Ceramic	0.01 µF, 35 V	R16(3)	General	Open
C9	Ceramic	0.01 µF, 35 V	R17(3)	General	Open
C10	Ceramic	0.1 µF, 35 V	R18(3)	General	Open
C11	Ceramic	1 µF, 35 V	R19	General	4.7k Ω, 1/8 W
C12	Ceramic	1 µF, 35 V	R20	General	Open
C13	Ceramic	1 µF, 35 V	R21	General	Open
C14	Ceramic	2200 pF, 35 V	R22(4)	General	Open
C15	Ceramic	1 µF, 50 V	R23	General	100 Ω, 1/8 W
C16	Ceramic	1 µF, 50 V	RS1	Metal plate	0.37 Ω, 1/8 W
C17	Ceramic	1 µF, 50 V	RS2	Metal plate	Open
CX1	Film	0.01 µF, 630 V	IC	IC	SX68128MB
R1(5)	General	Open	CN1	Pin header	Equiv. to B2P3-VH
R2(5)	General	Open	CN2	Pin header	Equiv. to B3P5-VH
R3(5)	General	Open	SV1	Connector	2.54 mm pitch pin header
R4(5)	General	Open	SV2	Connector	2.54 mm pitch pin header
R5(5)	General	Open	SV3	Connector	2.54 mm pitch pin header
R6(5)	General	Open			
R7(5)	General	Open			
R8(5)	General	Open			

(1) Should be connected when MLP = H and be left open when MLP = L.
(2) Should be connected when CW/CCW = H and be left open when CW/CCW = L.
(3) Should be connected for noise filtering.
(4) Refers to the setting value when f_{PWM} = 17 kHz (typ.).
(5) Should be connected when your application employs Hall IC inputs.

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